

**-20V(D-S) P-Channel Enhancement Mode Power MOS FET**

**General Features**

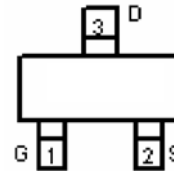
- $V_{DS} = -20V, I_D = -4.1A$   
 $R_{DS(ON)} < 75m\Omega @ V_{GS} = -2.5V$   
 $R_{DS(ON)} < 52m\Omega @ V_{GS} = -4.5V$
- High power and current handling capability
- Lead free product is acquired
- Surface mount package



**Lead Free**

**Application**

- PWM applications
- Load switch
- Power management

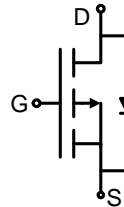


**Marking and pin assignment**

**PIN Configuration**



**SOT-23 top view**



**Schematic diagram**

**Package Marking and Ordering Information**

Device Marking	Device	Device Package	Reel Size	Tape width	Quantity
	MSP0205	SOT-23	Ø180mm	8 mm	3000 units

**Absolute Maximum Ratings ( $T_A = 25^\circ C$  unless otherwise noted)**

Parameter		Symbol	Limit	Unit
Drain-Source Voltage		$V_{DS}$	-20	V
Gate-Source Voltage		$V_{GS}$	$\pm 12$	V
Continuous Drain Current	$T_C = 25^\circ C$	$I_D$	-4.1	A
	$T_C = 70^\circ C$		-3.2	
	$T_A = 25^\circ C$		-3	
	$T_A = 70^\circ C$		-2.3	
Drain Current -Pulsed (Note 1)		$I_{DM}$	-15	A
Maximum Power Dissipation		$P_D$	1.7	W
Operating Junction and Storage Temperature Range		$T_J, T_{STG}$	-55 To 150	$^\circ C$

**Thermal Characteristic**

Thermal Resistance, Junction-to-Ambient (Note 2)	$R_{\theta JA}$	74	$^\circ C/W$
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**Electrical Characteristics (T<sub>A</sub>=25°C unless otherwise noted)**

Parameter	Symbol	Condition	Min	Typ	Max	Unit
<b>Off Characteristics</b>						
Drain-Source Breakdown Voltage	BV <sub>DSS</sub>	V <sub>GS</sub> =0V I <sub>D</sub> =-250μA	-20	-	-	V
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>DS</sub> =-20V, V <sub>GS</sub> =0V	-	-	-1	μA
Gate-Body Leakage Current	I <sub>GSS</sub>	V <sub>GS</sub> =±12V, V <sub>DS</sub> =0V	-	-	±100	nA
<b>On Characteristics (Note 3)</b>						
Gate Threshold Voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> =V <sub>GS</sub> , I <sub>D</sub> =-250μA	-0.45	-0.7	-1.0	V
Drain-Source On-State Resistance	R <sub>DS(ON)</sub>	V <sub>GS</sub> =-4.5V, I <sub>D</sub> =-4.1A	-	39	52	mΩ
		V <sub>GS</sub> =-2.5V, I <sub>D</sub> =-3A	-	58	75	
Forward Transconductance	g <sub>FS</sub>	V <sub>DS</sub> =-5V, I <sub>D</sub> =-2A	6	-	-	S
<b>Dynamic Characteristics (Note4)</b>						
Input Capacitance	C <sub>ISS</sub>	V <sub>DS</sub> =-4V, V <sub>GS</sub> =0V, F=1.0MHz	-	740	-	PF
Output Capacitance	C <sub>OSS</sub>		-	290	-	PF
Reverse Transfer Capacitance	C <sub>RSS</sub>		-	190	-	PF
<b>Switching Characteristics (Note 4)</b>						
Turn-on Delay Time	t <sub>d(on)</sub>	V <sub>DD</sub> =-4V, I <sub>D</sub> =-3.3A , R <sub>L</sub> =-1.2Ω, V <sub>GEN</sub> =-4.5V, R <sub>g</sub> =1Ω	-	12	-	nS
Turn-on Rise Time	t <sub>r</sub>		-	35	-	nS
Turn-Off Delay Time	t <sub>d(off)</sub>		-	30	-	nS
Turn-Off Fall Time	t <sub>f</sub>		-	10	-	nS
Total Gate Charge	Q <sub>g</sub>	V <sub>DS</sub> =-4V, I <sub>D</sub> =-4.1A, V <sub>GS</sub> =-4.5V	-	7.8	-	nC
Gate-Source Charge	Q <sub>gs</sub>		-	1.2	-	nC
Gate-Drain Charge	Q <sub>gd</sub>		-	1.6	-	nC
<b>Drain-Source Diode Characteristics</b>						
Diode Forward Voltage (Note 3)	V <sub>SD</sub>	V <sub>GS</sub> =0V, I <sub>S</sub> =-1.6A	-	-	-1.2	V
Diode Forward Current (Note 2)	I <sub>S</sub>		-	-	1.6	A

**Notes:**

1. Repetitive Rating: Pulse width limited by maximum junction temperature.
2. Surface Mounted on FR4 Board, t ≤ 10 sec.
3. Pulse Test: Pulse Width ≤ 300μs, Duty Cycle ≤ 2%.
4. Guaranteed by design, not subject to production

Typical Electrical and Thermal Characteristics

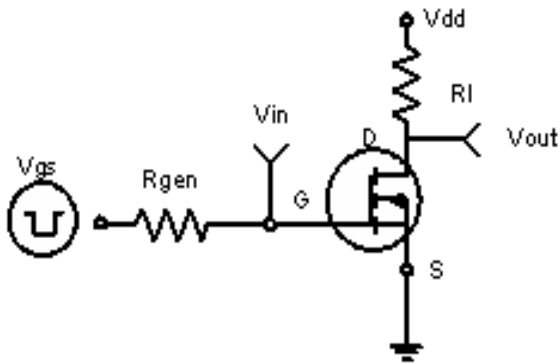


Figure 1: Switching Test Circuit

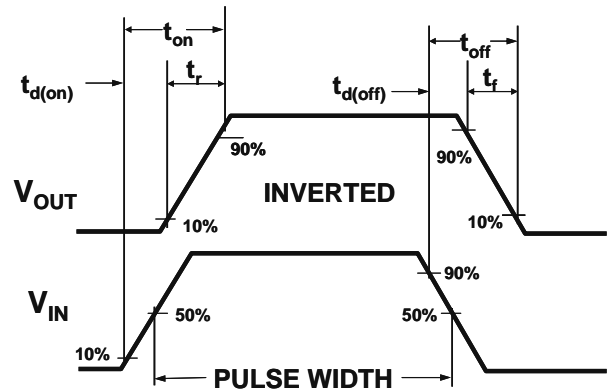
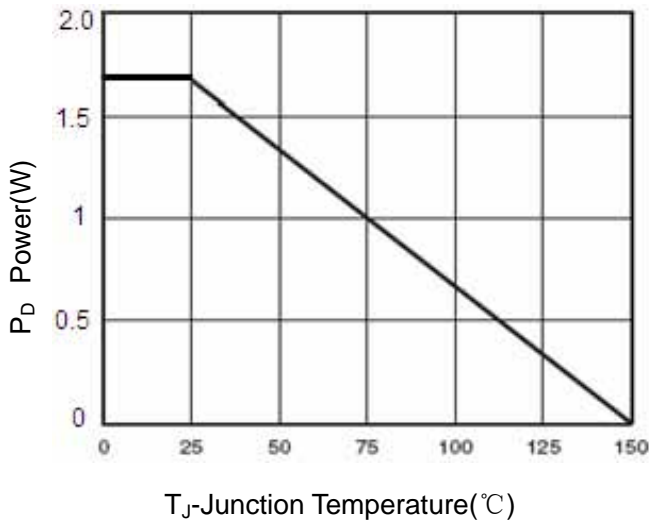
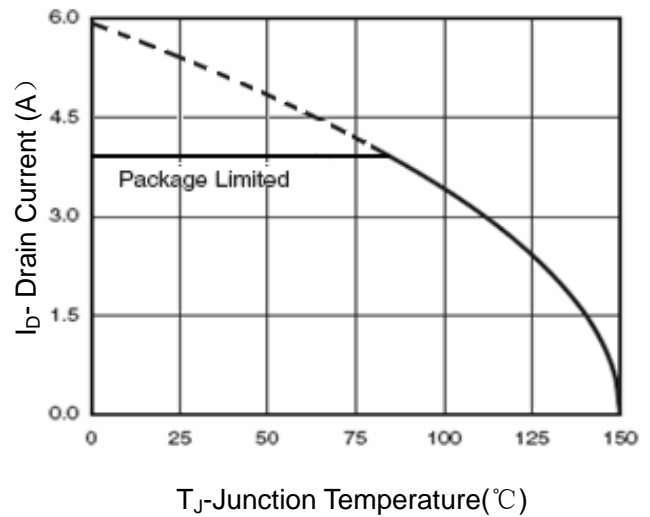


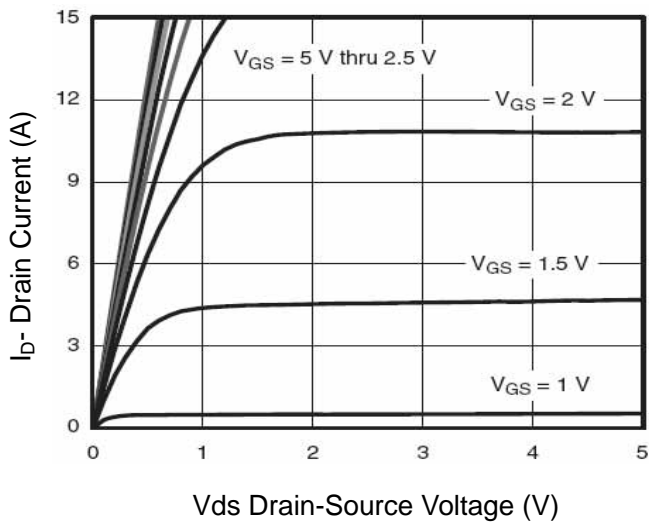
Figure 2: Switching Waveforms



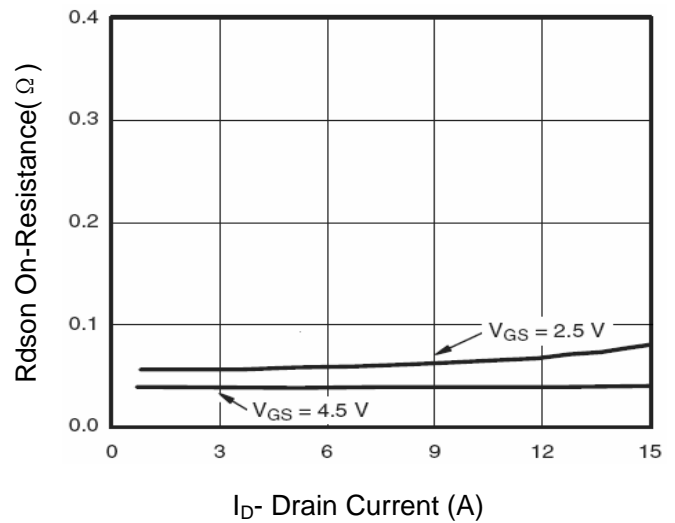
T<sub>J</sub>-Junction Temperature(°C)  
Figure 3 Power Dissipation



T<sub>J</sub>-Junction Temperature(°C)  
Figure 4 Drain Current



V<sub>ds</sub> Drain-Source Voltage (V)  
Figure 5 Output Characteristics



I<sub>D</sub>- Drain Current (A)  
Figure 6 Drain-Source On-Resistance

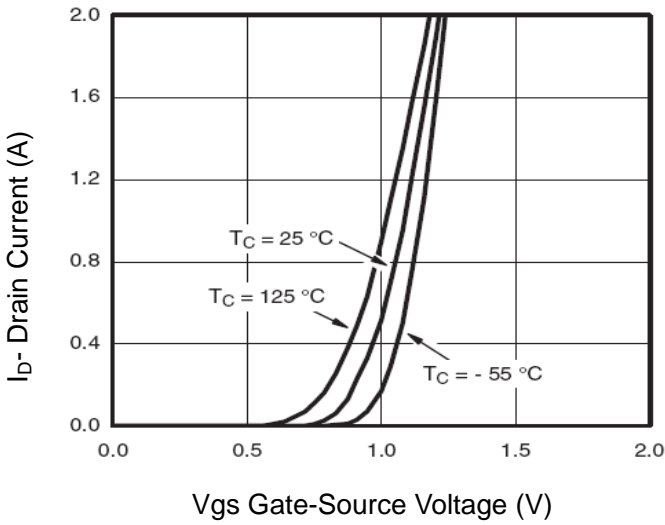


Figure 7 Transfer Characteristics

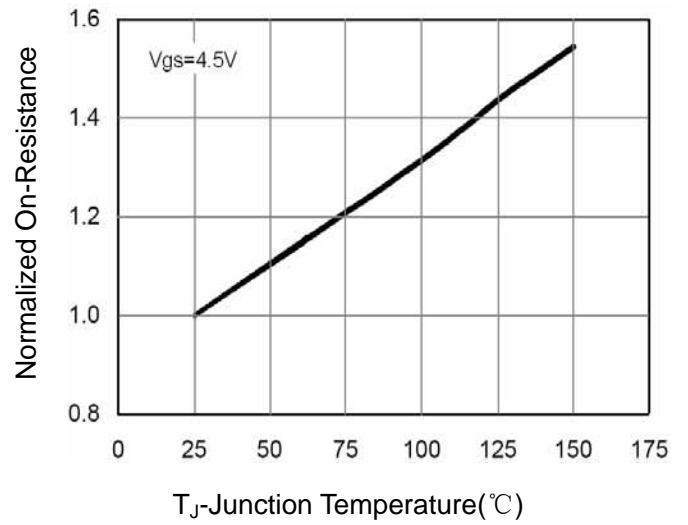


Figure 8 Drain-Source On-Resistance

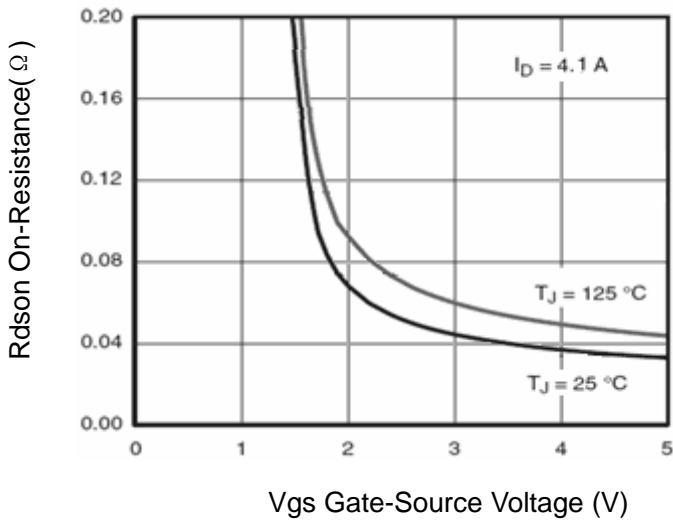


Figure 9 Rdson vs Vgs

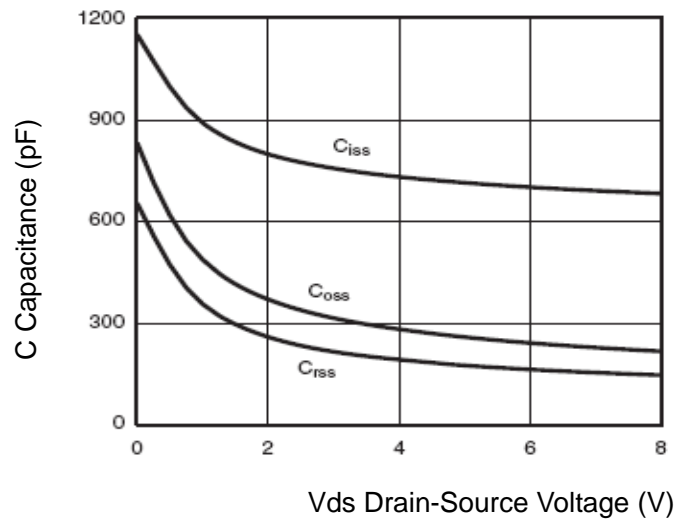


Figure 10 Capacitance vs Vds

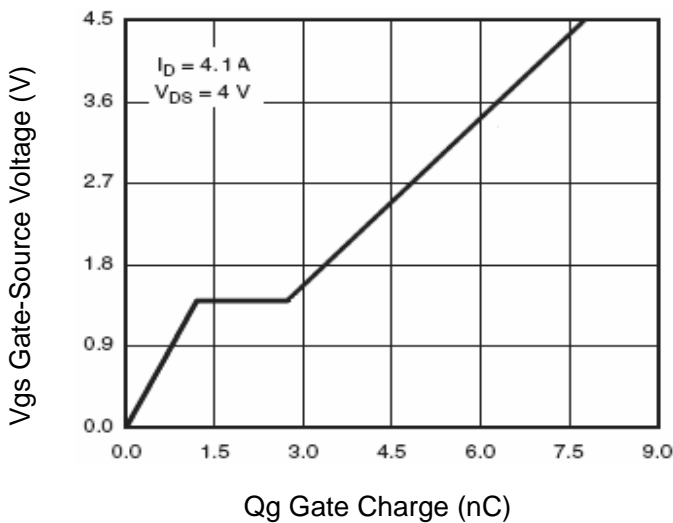


Figure 11 Gate Charge

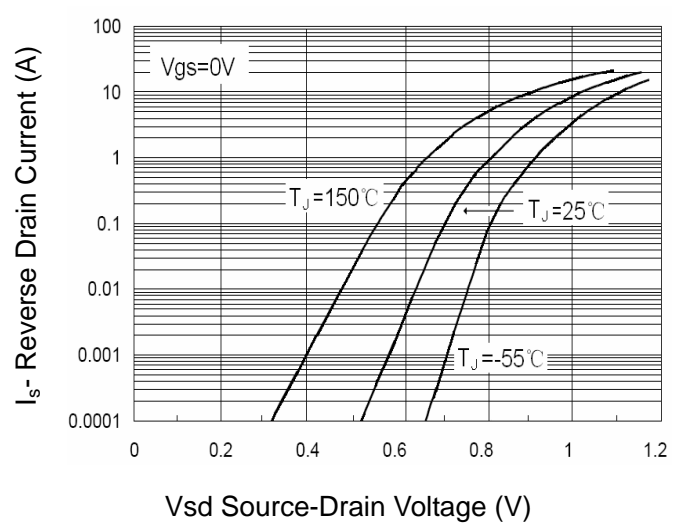


Figure 12 Source- Drain Diode Forward

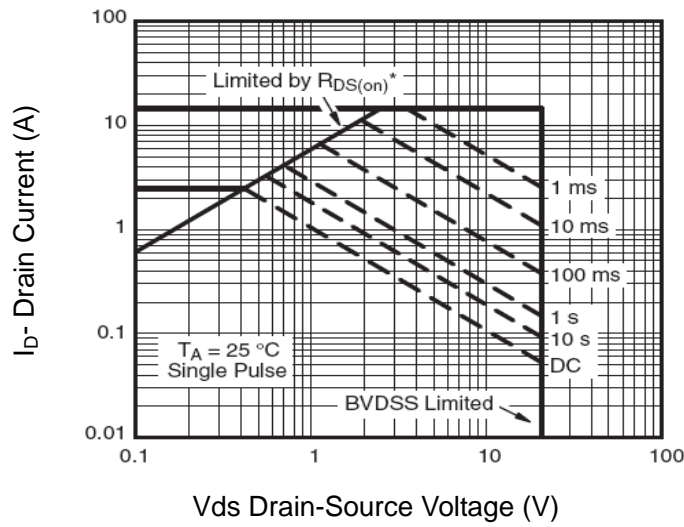


Figure 13 Safe Operation Area

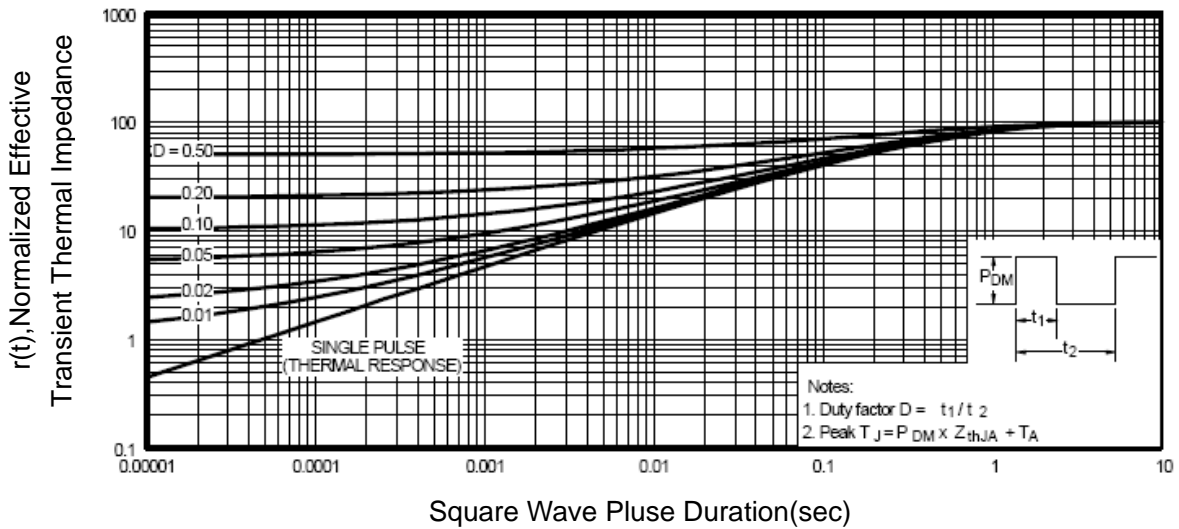
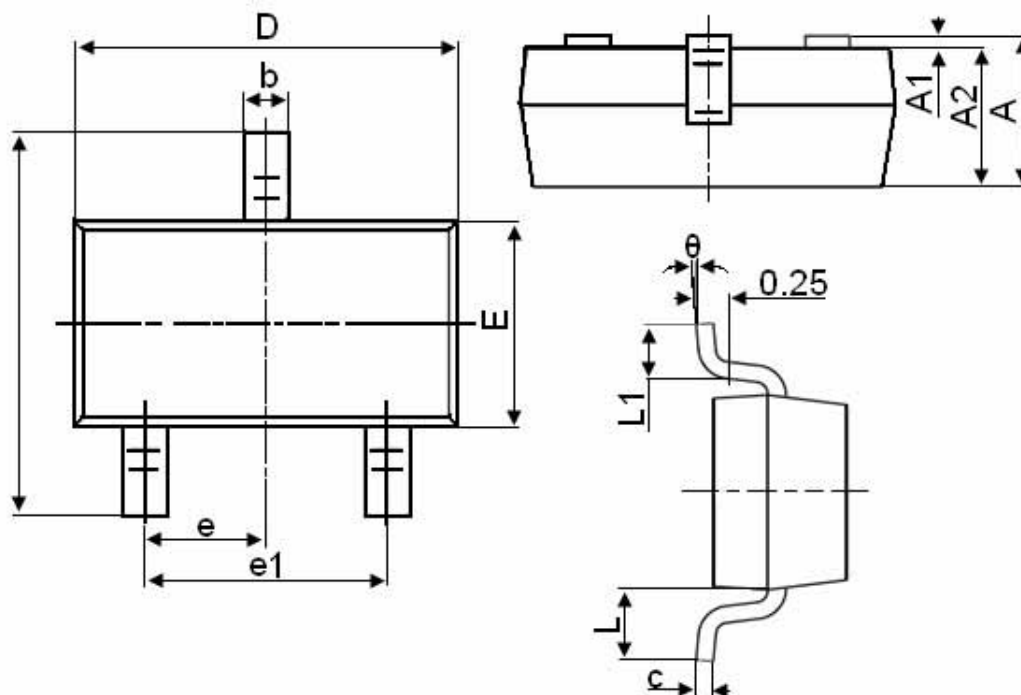


Figure 14 Normalized Maximum Transient Thermal Impedance

**SOT-23 Package Information**



Symbol	Dimensions in Millimeters	
	MIN.	MAX.
A	0.900	1.150
A1	0.000	0.100
A2	0.900	1.050
b	0.300	0.500
c	0.080	0.150
D	2.800	3.000
E	1.200	1.400
E1	2.250	2.550
e	0.950TYP	
e1	1.800	2.000
L	0.550REF	
L1	0.300	0.500
θ	0°	8°

**Notes**

1. All dimensions are in millimeters.
2. Tolerance  $\pm 0.10\text{mm}$  (4 mil) unless otherwise specified
3. Package body sizes exclude mold flash and gate burrs. Mold flash at the non-lead sides should be less than 5 mils.
4. Dimension L is measured in gauge plane.
5. Controlling dimension is millimeter, converted inch dimensions are not necessarily exact.