

**600V(D-S) N-Channel Enhancement Mode Power MOS FET**

**General Features**

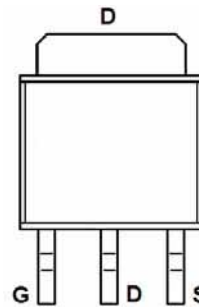
- $V_{DS} = 600V, I_D = 2A$   
 $R_{DS(ON)} < 5.0 \Omega @ V_{GS} = 10V$
- High density cell design for ultra low  $R_{dson}$
- Fully characterized avalanche voltage and current
- Good stability and uniformity with high  $E_{AS}$
- Excellent package for good heat dissipation
- Special process technology for high ESD capability



**Lead Free**

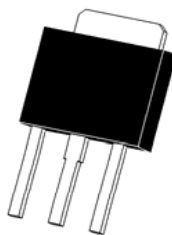
**Application**

- Power switching application
- Hard switched and high frequency circuits
- Uninterruptible power supply

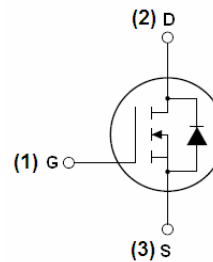


**Marking and pin assignment**

**PIN Configuration**



**TO-251 top view**



**Schematic diagram**

**Package Marking and Ordering Information**

Device Marking	Device	Device Package	Reel Size	Tape width	Quantity
MSN6002Z	MSN6002Z	TO-251	-	-	-

**Absolute Maximum Ratings ( $T_C = 25^\circ C$  unless otherwise noted)**

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	$V_{DS}$	600	V
Gate-Source Voltage	$V_{GS}$	$\pm 30$	V
Drain Current-Continuous	$I_D$	2	A
Drain Current-Continuous( $T_C = 100^\circ C$ )	$I_D(100^\circ C)$	1.35	A
Pulsed Drain Current	$I_{DM}$	6	A
Maximum Power Dissipation	$P_D$	44	W
Derating factor		0.28	W/ $^\circ C$
Single pulse avalanche energy <sup>(Note 5)</sup>	$E_{AS}$	141	mJ
Operating Junction and Storage Temperature Range	$T_J, T_{STG}$	-55 To 150	$^\circ C$

**Thermal Characteristic**

Thermal Resistance, Junction-to-Case <sup>(Note 2)</sup>	$R_{\theta JC}$	5.5	$^{\circ}C/W$
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**Electrical Characteristics ( $T_C=25^{\circ}C$  unless otherwise noted)**

Parameter	Symbol	Condition	Min	Typ	Max	Unit
<b>Off Characteristics</b>						
Drain-Source Breakdown Voltage	$BV_{DSS}$	$V_{GS}=0V, I_D=250\mu A$	600	-	-	V
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS}=600V, V_{GS}=0V$	-	-	25	$\mu A$
Gate-Body Leakage Current	$I_{GSS}$	$V_{GS}=\pm 30V, V_{DS}=0V$	-	-	$\pm 100$	nA
<b>On Characteristics</b> <sup>(Note 3)</sup>						
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=250\mu A$	2	-	4	V
Drain-Source On-State Resistance	$R_{DS(on)}$	$V_{GS}=10V, I_D=1.0A$	-	-	5.0	$\Omega$
Forward Transconductance	$g_{FS}$	$V_{DS}=40V, I_D=1.0A$	-	2.45	-	S
<b>Dynamic Characteristics</b> <sup>(Note 4)</sup>						
Input Capacitance	$C_{iss}$	$V_{DS}=25V, V_{GS}=0V,$ $F=1.0MHz$	-	315	-	PF
Output Capacitance	$C_{oss}$		-	38	-	PF
Reverse Transfer Capacitance	$C_{rss}$		-	14	-	PF
<b>Switching Characteristics</b> <sup>(Note 4)</sup>						
Turn-on Delay Time	$t_{d(on)}$	$V_{DD}=300V, I_D=2A, R_L=25\Omega$ $V_{GS}=10V, R_G=2.5\Omega$	-	12	-	nS
Turn-on Rise Time	$t_r$		-	15	-	nS
Turn-Off Delay Time	$t_{d(off)}$		-	41	-	nS
Turn-Off Fall Time	$t_f$		-	16	-	nS
Total Gate Charge	$Q_g$	$V_{DS}=480V, I_D=2A,$ $V_{GS}=10V$	-	15	-	nC
Gate-Source Charge	$Q_{gs}$		-	2.6	-	nC
Gate-Drain Charge	$Q_{gd}$		-	6.7	-	nC
<b>Drain-Source Diode Characteristics</b>						
Diode Forward Voltage <sup>(Note 3)</sup>	$V_{SD}$	$V_{GS}=0V, I_S=2.0A$	-	-	1.4	V
Diode Forward Current <sup>(Note 2)</sup>	$I_S$		-	-	2.0	A
Reverse Recovery Time	$t_{rr}$	$T_J = 25^{\circ}C, I_F = 2.0A$ $di/dt = 100A/\mu s$ <sup>(Note 3)</sup>	-	180	-	nS
Reverse Recovery Charge	$Q_{rr}$		-	0.72	-	$\mu C$
Forward Turn-On Time	$t_{on}$	Intrinsic turn-on time is negligible (turn-on is dominated by LS+LD)				

**Notes:**

1. Repetitive Rating: Pulse width limited by maximum junction temperature.
2. Surface Mounted on FR4 Board,  $t \leq 10$  sec.
3. Pulse Test: Pulse Width  $\leq 300\mu s$ , Duty Cycle  $\leq 2\%$ .
4. Guaranteed by design, not subject to production
5.  $E_{AS}$  condition:  $j=25^{\circ}C, V_{DD}=50V, V_G=10V, L=0.5mH, R_g=25\Omega$

Typical Electrical and Thermal Characteristics (Curves)

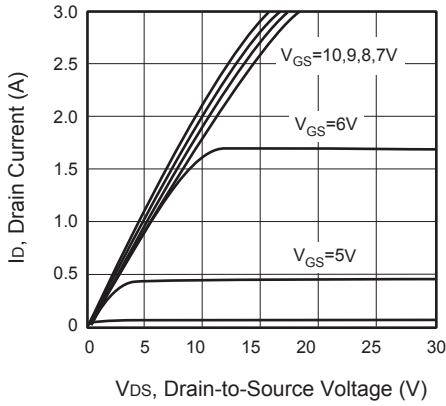


Figure 1. Output Characteristics

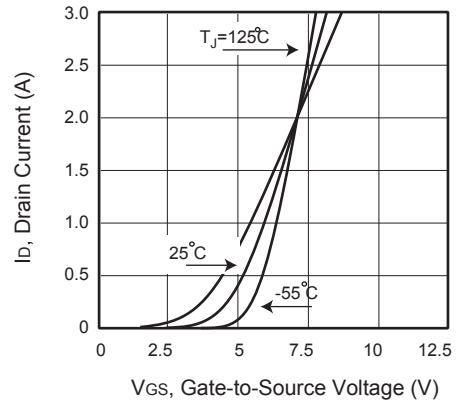


Figure 2. Transfer Characteristics

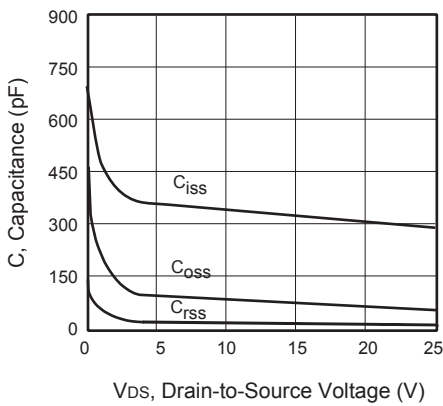


Figure 3. Capacitance

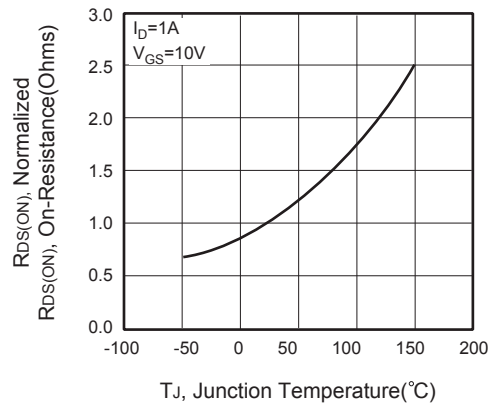


Figure 4. On-Resistance Variation with Temperature

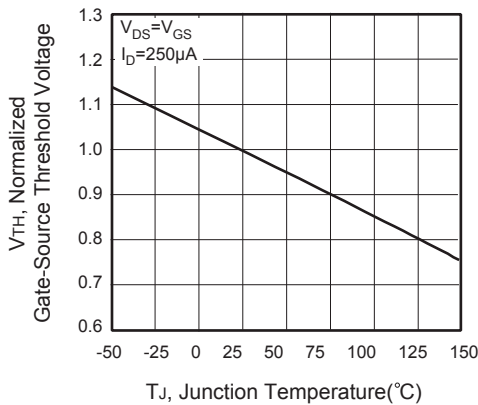


Figure 5. Gate Threshold Variation with Temperature

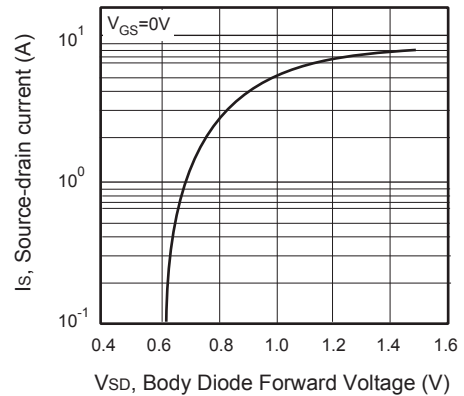


Figure 6. Body Diode Forward Voltage Variation with Source Current

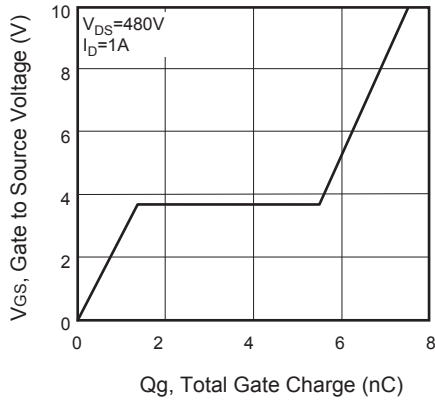


Figure 7. Gate Charge

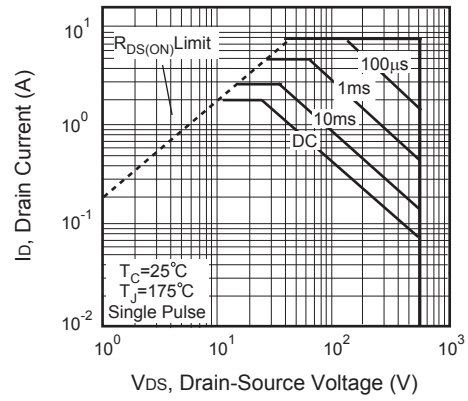


Figure 8. Maximum Safe Operating Area

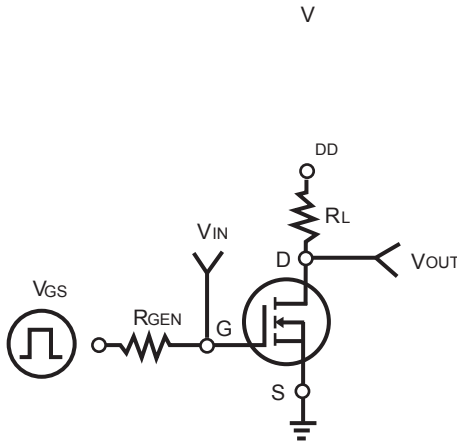


Figure 9. Switching Test Circuit

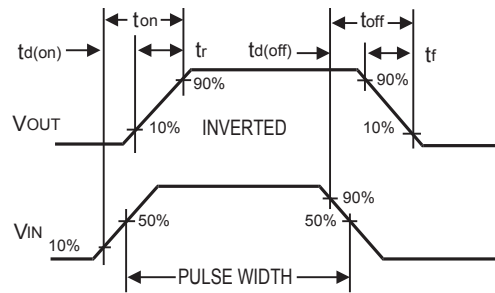


Figure 10. Switching Waveforms

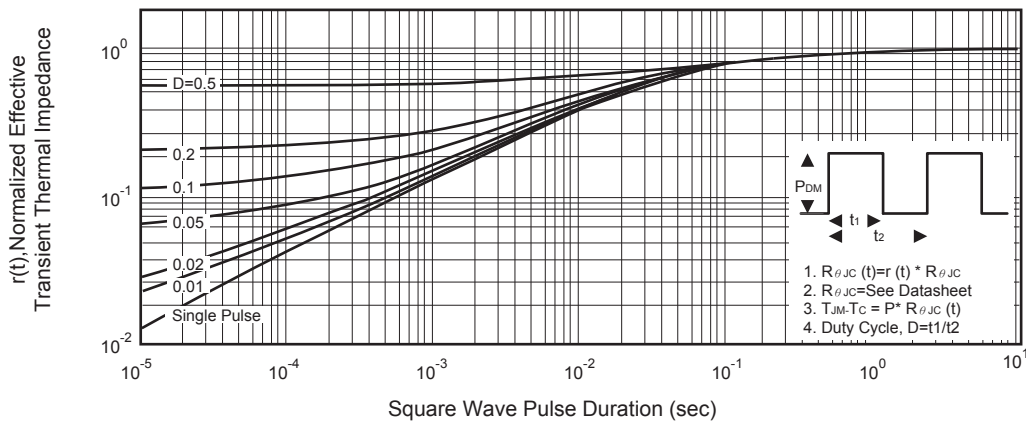
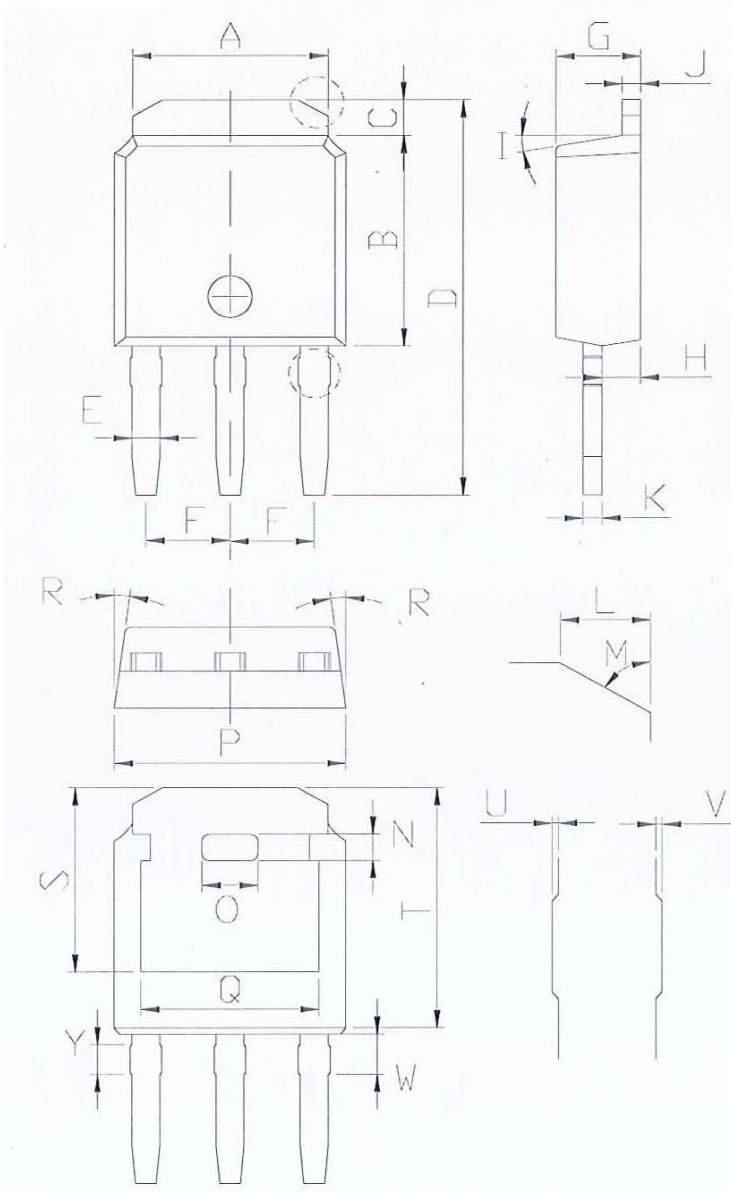


Figure 11. Normalized Thermal Transient Impedance Curve

**TO-251 Package Information**



DIM	MILLIMETERS
A	5.34±0.30
B	6.00±0.30
C	1.05±0.30
D	11.31±0.30
E	0.76±0.15
F	2.28±0.15
G	2.30±0.30
H	1.06±0.30
I	(4-10)°
J	0.51±0.15
K	0.52±0.15
L	0.80±0.30
M	60°
N	0.75±0.30
O	1.80±0.30
P	6.60±0.30
Q	4.85±0.30
R	(4-8.5)°
S	5.30±0.30
T	6.90±0.30
U	0.05±0.05
V	0.05±0.05
W	1.15±0.25
Y	0.85±0.25