

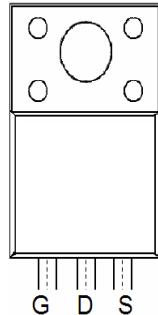
## 600V(D-S) N-Channel Enhancement Mode Power MOS FET

### General Features

- $V_{DS} = 600V, I_D = 2A$
- $R_{DS(ON)} < 5.0 \Omega @ V_{GS}=10V$
- High density cell design for ultra low  $R_{DS(on)}$
- Fully characterized avalanche voltage and current
- Good stability and uniformity with high  $E_{AS}$
- Excellent package for good heat dissipation
- Special process technology for high ESD capability

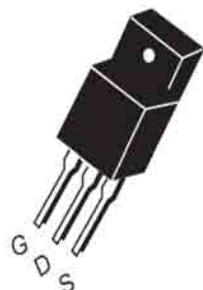


**Lead Free**

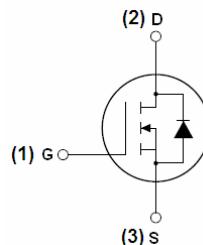


**Marking and pin assignment**

### PIN Configuration



**TO-220F top view**



**Schematic diagram**

### Package Marking and Ordering Information

Device Marking	Device	Device Package	Reel Size	Tape width	Quantity
MSN6002F	MSN6002F	TO-220F-3L	-	-	-

### Absolute Maximum Ratings ( $T_C=25^\circ\text{C}$ unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	$V_{DS}$	600	V
Gate-Source Voltage	$V_{GS}$	$\pm 30$	V
Drain Current-Continuous	$I_D$	2	A
Drain Current-Continuous( $T_C=100^\circ\text{C}$ )	$I_D (100^\circ\text{C})$	1.35	A
Pulsed Drain Current	$I_{DM}$	6	A
Maximum Power Dissipation	$P_D$	35	W
Derating factor		0.28	$W/\text{^\circ C}$
Single pulse avalanche energy (Note 5)	$E_{AS}$	240	mJ
Operating Junction and Storage Temperature Range	$T_J, T_{STG}$	-55 To 150	$^\circ\text{C}$

### Thermal Characteristic

Thermal Resistance, Junction-to-Case <sup>(Note 2)</sup>	R <sub>θJC</sub>	5.5	°C/W
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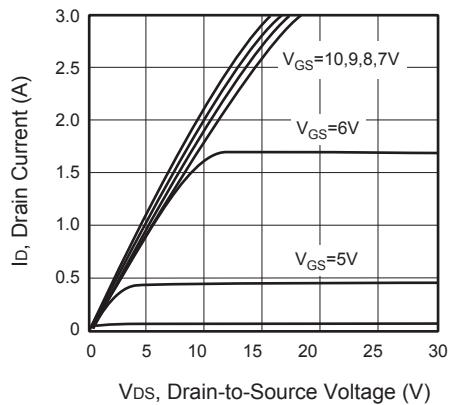
### Electrical Characteristics (T<sub>C</sub>=25°C unless otherwise noted)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
<b>Off Characteristics</b>						
Drain-Source Breakdown Voltage	BV <sub>DSS</sub>	V <sub>GS</sub> =0V, I <sub>D</sub> =250μA	600	-	-	V
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>DS</sub> =600V, V <sub>GS</sub> =0V	-	-	1	μA
Gate-Body Leakage Current	I <sub>GSS</sub>	V <sub>GS</sub> =±30V, V <sub>DS</sub> =0V	-	-	±100	nA
<b>On Characteristics</b> <sup>(Note 3)</sup>						
Gate Threshold Voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> =V <sub>GS</sub> , I <sub>D</sub> =250μA	2	-	4	V
Drain-Source On-State Resistance	R <sub>DS(ON)</sub>	V <sub>GS</sub> =10V, I <sub>D</sub> =1.0A	-	-	5.0	Ω
Forward Transconductance	g <sub>F</sub>	V <sub>DS</sub> =40V, I <sub>D</sub> =1.0A	-	2.05	-	S
<b>Dynamic Characteristics</b> <sup>(Note 4)</sup>						
Input Capacitance	C <sub>iss</sub>	V <sub>DS</sub> =25V, V <sub>GS</sub> =0V, F=1.0MHz	-	190	-	PF
Output Capacitance	C <sub>oss</sub>		-	15	-	PF
Reverse Transfer Capacitance	C <sub>rss</sub>		-	1.8	-	PF
<b>Switching Characteristics</b> <sup>(Note 4)</sup>						
Turn-on Delay Time	t <sub>d(on)</sub>	V <sub>DD</sub> =300V, I <sub>D</sub> =2A, R <sub>L</sub> =25Ω V <sub>GS</sub> =10V, R <sub>G</sub> =2.5Ω	-	7	-	nS
Turn-on Rise Time	t <sub>r</sub>		-	23	-	nS
Turn-Off Delay Time	t <sub>d(off)</sub>		-	22	-	nS
Turn-Off Fall Time	t <sub>f</sub>		-	24	-	nS
Total Gate Charge	Q <sub>g</sub>	V <sub>DS</sub> =480V, I <sub>D</sub> =2A, V <sub>GS</sub> =10V	-	5.3	-	nC
Gate-Source Charge	Q <sub>gs</sub>		-	1.8	-	nC
Gate-Drain Charge	Q <sub>gd</sub>		-	1.8	-	nC
<b>Drain-Source Diode Characteristics</b>						
Diode Forward Voltage <sup>(Note 3)</sup>	V <sub>SD</sub>	V <sub>GS</sub> =0V, I <sub>s</sub> =2.0A	-		1.4	V
Diode Forward Current <sup>(Note 2)</sup>	I <sub>s</sub>		-	-	2.0	A
Reverse Recovery Time	t <sub>rr</sub>	T <sub>J</sub> = 25°C, IF = 2.0A di/dt = 100A/μs <sup>(Note 3)</sup>	-	230	-	nS
Reverse Recovery Charge	Q <sub>rr</sub>		-	1.0	-	μC
Forward Turn-On Time	t <sub>on</sub>	Intrinsic turn-on time is negligible (turn-on is dominated by LS+LD)				

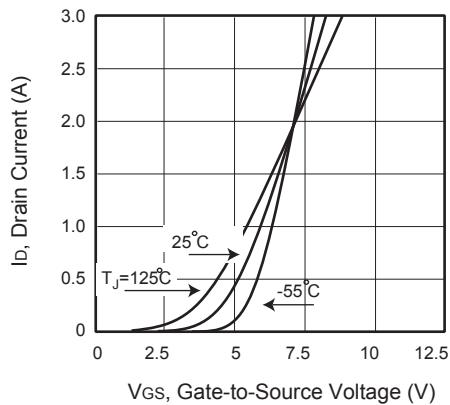
### Notes:

1. Repetitive Rating: Pulse width limited by maximum junction temperature.
  2. Surface Mounted on FR4 Board, t ≤ 10 sec.
  3. Pulse Test: Pulse Width ≤ 300μs, Duty Cycle ≤ 2%.
  4. Guaranteed by design, not subject to production
5. E<sub>AS</sub> condition: j=25°C, V<sub>DD</sub>=50V, V<sub>G</sub>=10V, L=0.5mH, R<sub>G</sub>=25Ω

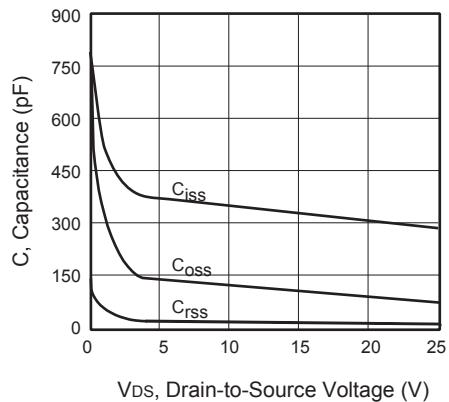
### Typical Electrical and Thermal Characteristics (Curves)



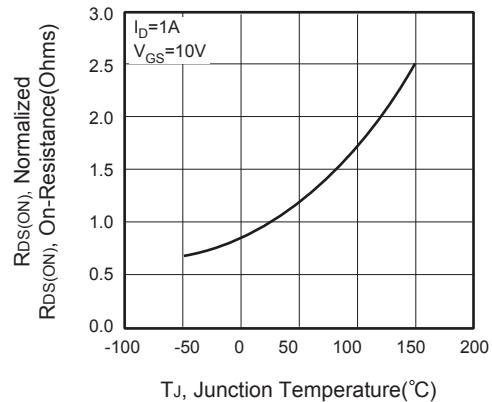
**Figure 1. Output Characteristics**



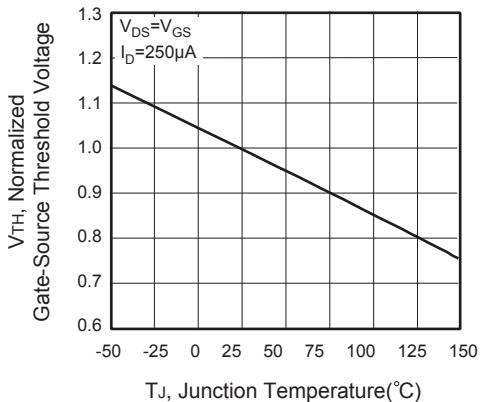
**Figure 2. Transfer Characteristics**



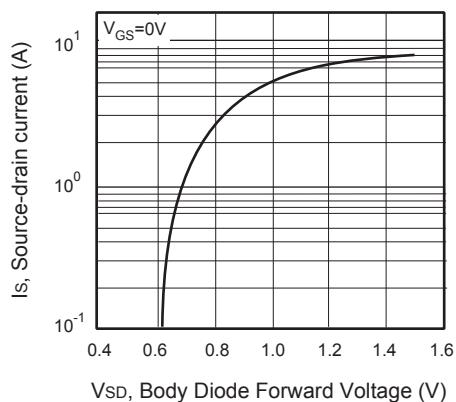
**Figure 3. Capacitance**



**Figure 4. On-Resistance Variation with Temperature**



**Figure 5. Gate Threshold Variation with Temperature**



**Figure 6. Body Diode Forward Voltage Variation with Source Current**

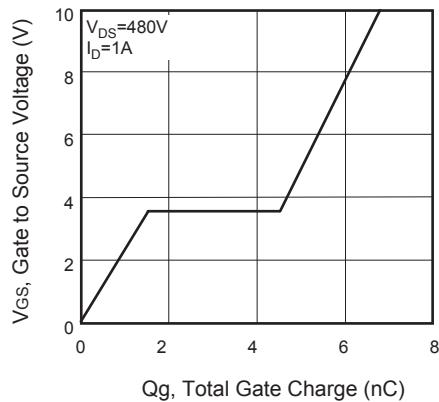


Figure 7. Gate Charge

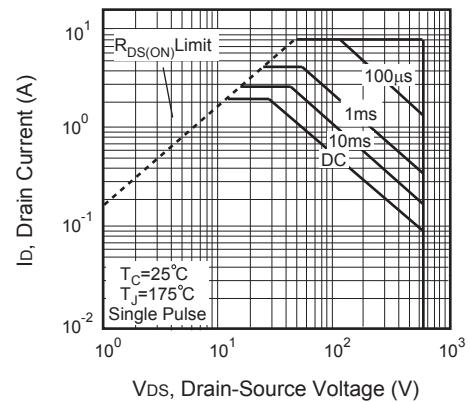


Figure 8. Maximum Safe  
Operating Area

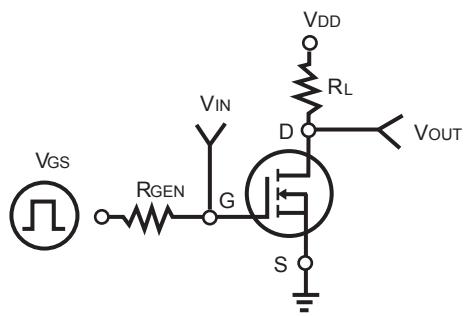


Figure 9. Switching Test Circuit

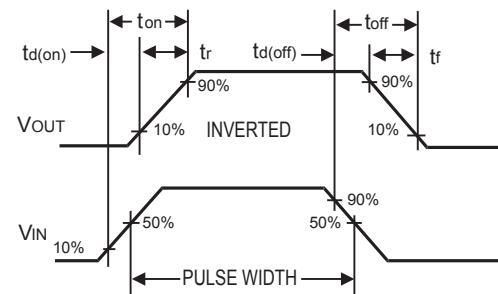


Figure 10. Switching Waveforms

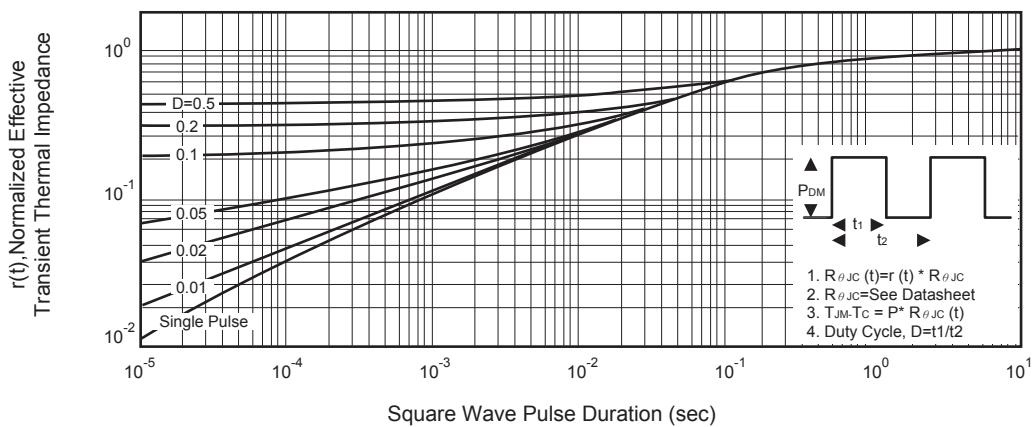
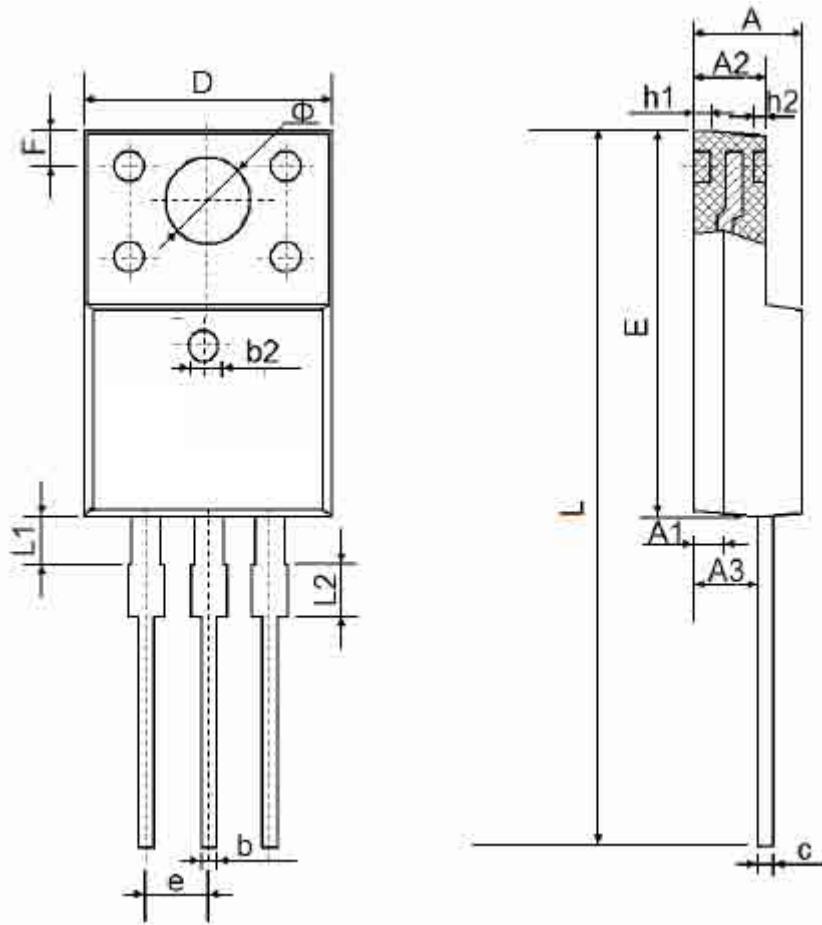


Figure 11. Normalized Thermal Transient Impedance Curve

TO-220F-3L Package Information



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	4.300	4.700	0.169	0.185
A1	1.300REF		0.051REF	
A2	2.800	3.200	0.110	0.126
A3	2.500	2.900	0.098	0.114
b	0.500	0.750	0.020	0.030
b1	1.100	1.350	0.043	0.053
b2	1.500	1.750	0.059	0.069
c	0.500	0.750	0.020	0.030
D	9.960	10.360	0.392	0.408
E	14.800	15.200	0.583	0.598
e	2.540TYP.		0.100TYP	
F	2.700REF		0.106REF	
Φ	3.500REF		0.138REF	
h1	0.800REF		0.031REF	
h2	0.500REF		0.020REF	
L	28.000	28.400	1.102	1.118
L1	1.700	1.900	0.067	0.075
L2	1.900	2.100	0.075	0.083