

**150V(D-S) N-Channel Enhancement Mode Power MOS FET**

**General Features**

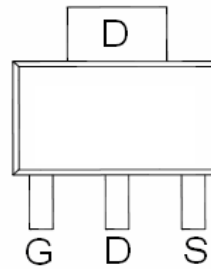
- $V_{DS} = 150V, I_D = 2A$   
 $R_{DS(ON)} < 300m\Omega @ V_{GS}=10V$  (Typ:260m $\Omega$ )
- High density cell design for ultra low  $R_{dson}$
- Fully characterized avalanche voltage and current
- Excellent package for good heat dissipation



**Lead Free**

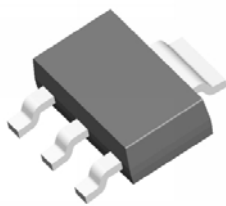
**Application**

- Power switching application
- Hard switched and high frequency circuits

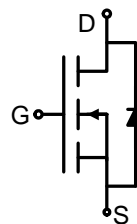


**Marking and pin assignment**

**PIN Configuration**



**SOT-223-3L view**



**Schematic diagram**

**Package Marking and Ordering Information**

Device Marking	Device	Device Package	Reel Size	Tape width	Quantity
MSN1502U	MSN1502U	SOT-223-3L	Ø330mm	12mm	2500 units

**Absolute Maximum Ratings ( $T_A=25^{\circ}C$  unless otherwise noted)**

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	$V_{DS}$	150	V
Gate-Source Voltage	$V_{GS}$	$\pm 20$	V
Drain Current-Continuous	$I_D$	2	A
Drain Current-Pulsed <sup>(Note 1)</sup>	$I_{DM}$	6	A
Maximum Power Dissipation	$P_D$	2	W
Operating Junction and Storage Temperature Range	$T_J, T_{STG}$	-55 To 150	$^{\circ}C$

**Thermal Characteristic**

Thermal Resistance, Junction-to-Ambient <sup>(Note 2)</sup>	$R_{\theta JA}$	62.5	$^{\circ}C/W$
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**Electrical Characteristics (T<sub>A</sub>=25°C unless otherwise noted)**

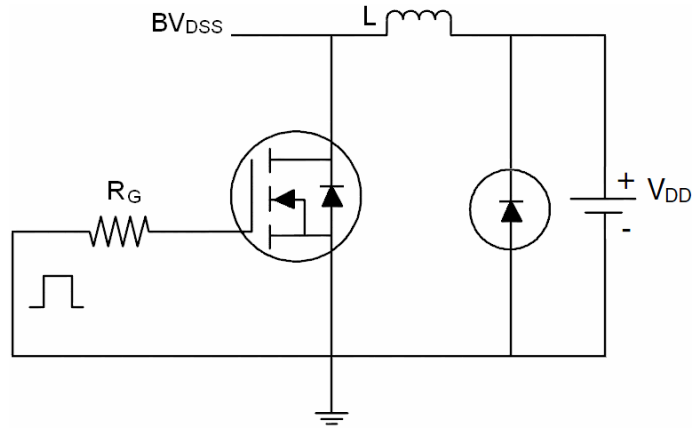
Parameter	Symbol	Condition	Min	Typ	Max	Unit
<b>Off Characteristics</b>						
Drain-Source Breakdown Voltage	BV <sub>DSS</sub>	V <sub>GS</sub> =0V I <sub>D</sub> =250μA	150	-	-	V
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>DS</sub> =150V, V <sub>GS</sub> =0V	-	-	1	μA
Gate-Body Leakage Current	I <sub>GSS</sub>	V <sub>GS</sub> =±20V, V <sub>DS</sub> =0V	-	-	±100	nA
<b>On Characteristics (Note 3)</b>						
Gate Threshold Voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> =V <sub>GS</sub> , I <sub>D</sub> =250μA	1.5	2.0	2.5	V
Drain-Source On-State Resistance	R <sub>DS(ON)</sub>	V <sub>GS</sub> =10V, I <sub>D</sub> =1.5A	-	260	300	mΩ
Forward Transconductance	g <sub>FS</sub>	V <sub>DS</sub> =15V, I <sub>D</sub> =1.5A	-	3	-	S
<b>Dynamic Characteristics (Note4)</b>						
Input Capacitance	C <sub>iss</sub>	V <sub>DS</sub> =25V, V <sub>GS</sub> =0V, F=1.0MHz	-	235	-	PF
Output Capacitance	C <sub>oss</sub>		-	36	-	PF
Reverse Transfer Capacitance	C <sub>rss</sub>		-	20	-	PF
<b>Switching Characteristics (Note 4)</b>						
Turn-on Delay Time	t <sub>d(on)</sub>	V <sub>DD</sub> =75V, I <sub>D</sub> =1A, R <sub>L</sub> =75Ω V <sub>GS</sub> =10V, R <sub>G</sub> =6Ω	-	8	-	nS
Turn-on Rise Time	t <sub>r</sub>		-	10	-	nS
Turn-Off Delay Time	t <sub>d(off)</sub>		-	20	-	nS
Turn-Off Fall Time	t <sub>f</sub>		-	15	-	nS
Total Gate Charge	Q <sub>g</sub>	V <sub>DS</sub> =75V, I <sub>D</sub> =1.5A, V <sub>GS</sub> =10V	-	8	-	nC
Gate-Source Charge	Q <sub>gs</sub>		-	1.4	-	nC
Gate-Drain Charge	Q <sub>gd</sub>		-	2.1	-	nC
<b>Drain-Source Diode Characteristics</b>						
Diode Forward Voltage (Note 3)	V <sub>SD</sub>	V <sub>GS</sub> =0V, I <sub>S</sub> =2A	-	-	1.2	V
Diode Forward Current (Note 2)	I <sub>S</sub>		-	-	2	A

**Notes:**

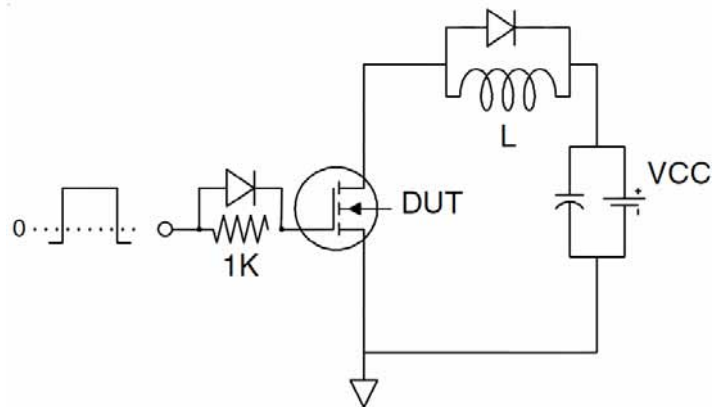
1. Repetitive Rating: Pulse width limited by maximum junction temperature.
2. Surface Mounted on FR4 Board, t ≤ 10 sec.
3. Pulse Test: Pulse Width ≤ 300μs, Duty Cycle ≤ 2%.
4. Guaranteed by design, not subject to product

**Test Circuit**

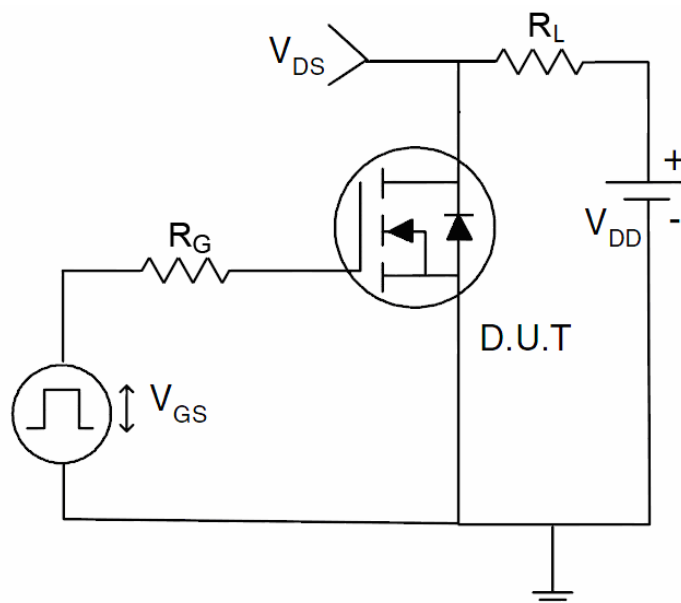
**1)  $E_{AS}$  Test Circuit**



**2) Gate Charge Test Circuit**



**3) Switch Time Test Circuit**



Typical Electrical and Thermal Characteristics (Curves)

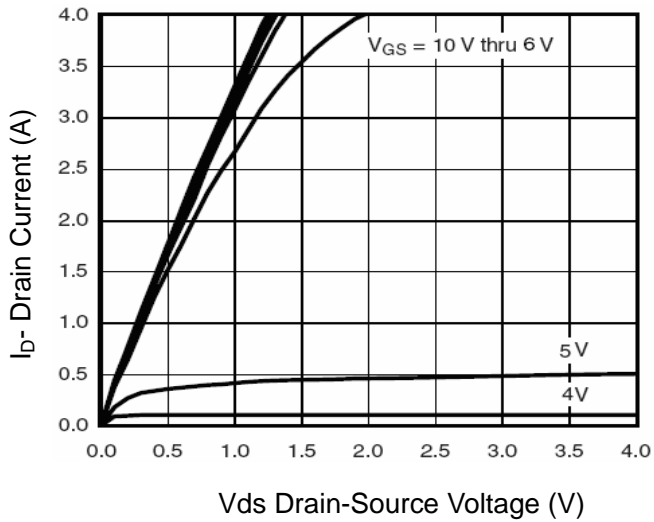


Figure 1 Output Characteristics

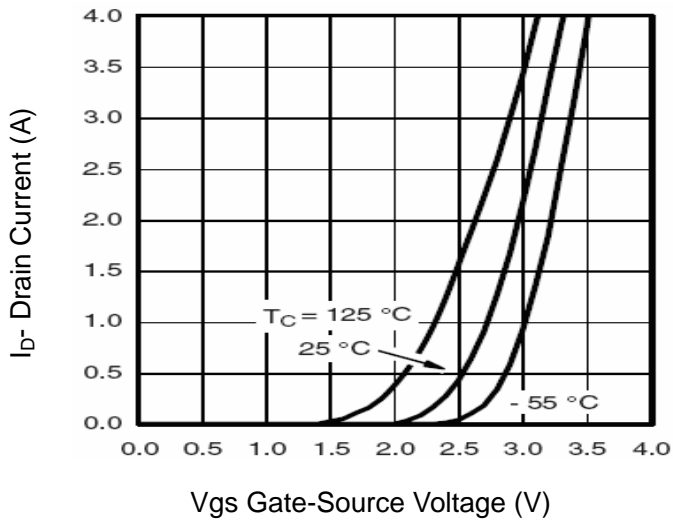


Figure 2 Transfer Characteristics

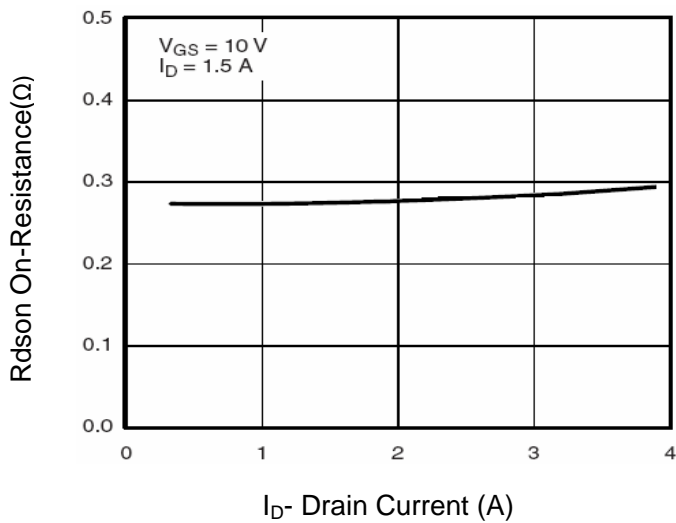


Figure 3  $R_{DS(on)}$ - Drain Current

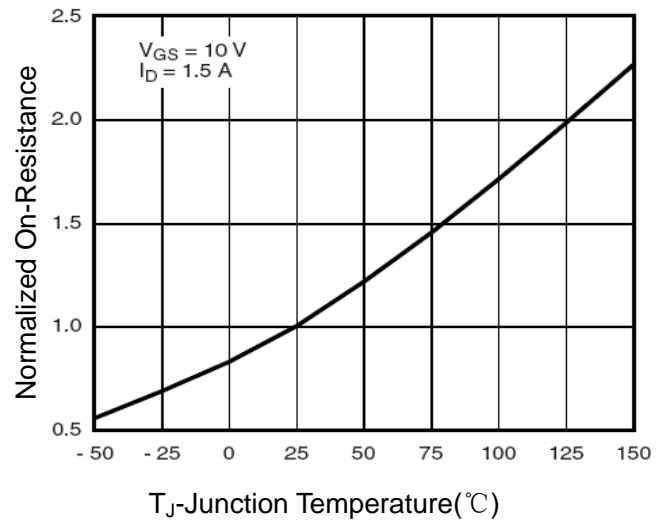


Figure 4  $R_{DS(on)}$ - Junction Temperature

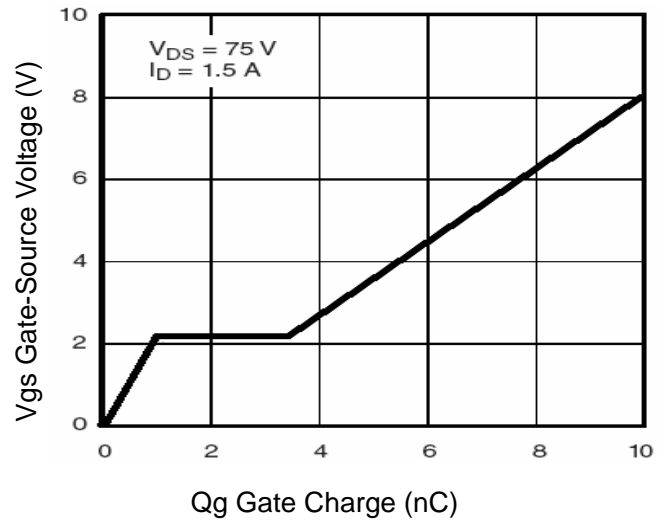


Figure 5 Gate Charge

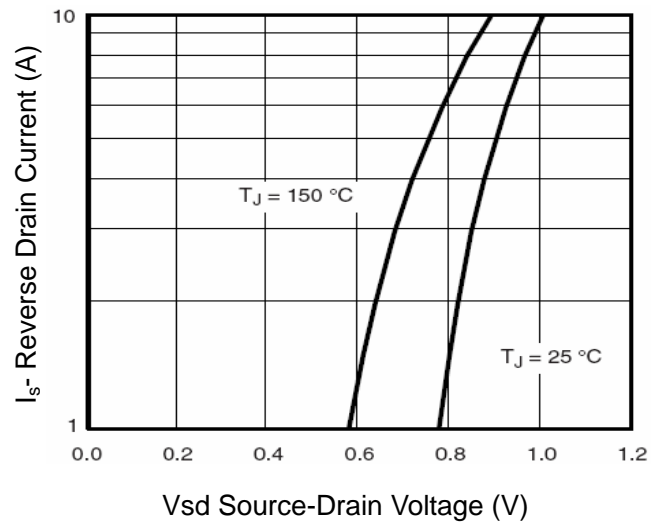


Figure 6 Source- Drain Diode Forward

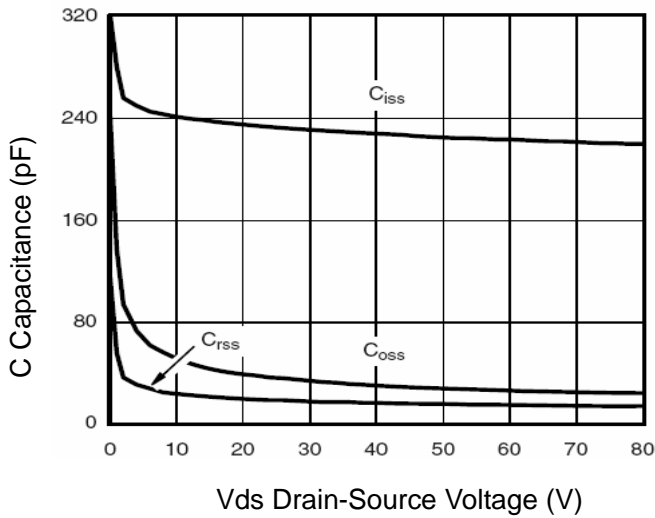


Figure 7 Capacitance vs Vds

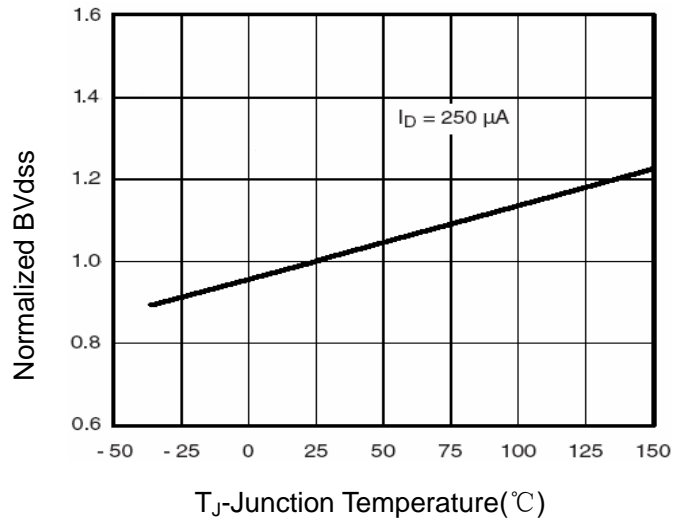


Figure 9  $BV_{DSS}$  vs Junction Temperature

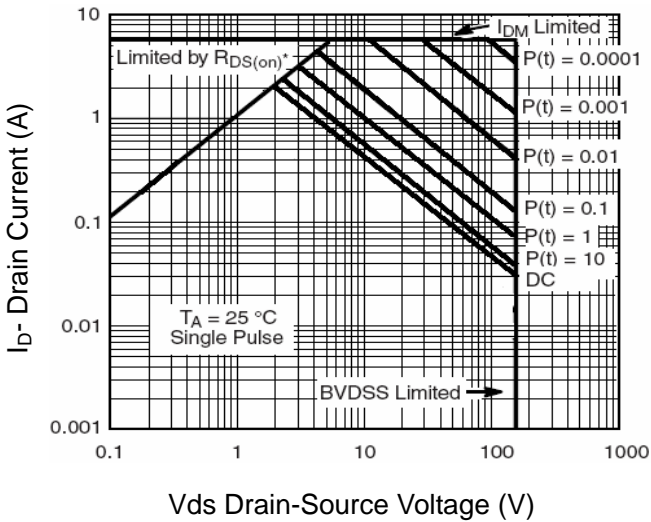


Figure 8 Safe Operation Area

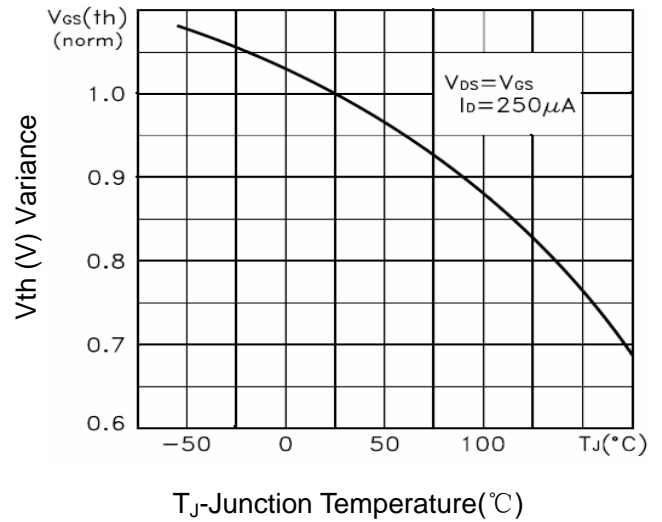


Figure 10  $V_{GS(th)}$  vs Junction Temperature

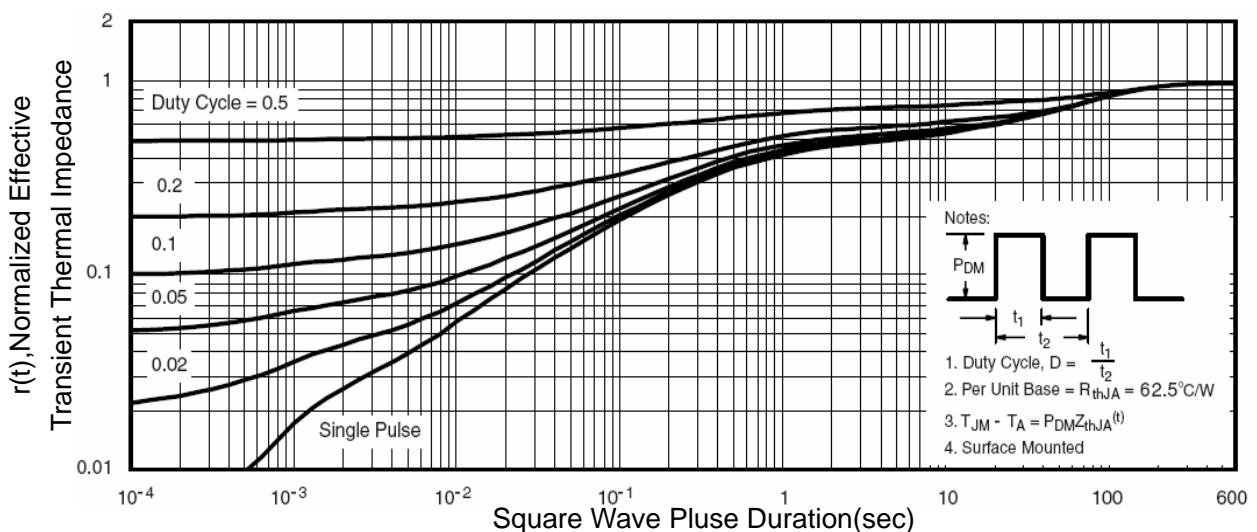
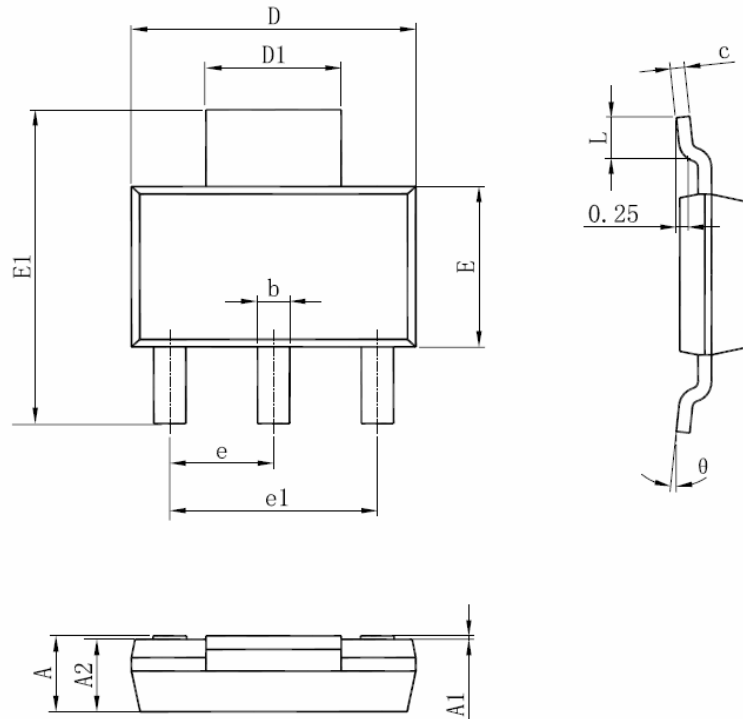


Figure 11 Normalized Maximum Transient Thermal Impedance

**SOT-223-3L Package Information**



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.520	1.800	0.060	0.071
A1	0.000	0.100	0.000	0.004
A2	1.500	1.700	0.059	0.067
b	0.660	0.820	0.026	0.032
c	0.250	0.350	0.010	0.014
D	6.200	6.400	0.244	0.252
D1	2.900	3.100	0.114	0.122
E	3.300	3.700	0.130	0.146
E1	6.830	7.070	0.269	0.278
e	2.300(BSC)		0.091(BSC)	
e1	4.500	4.700	0.177	0.185
L	0.900	1.150	0.035	0.045
θ	0°	10°	0°	10°

**Notes**

1. All dimensions are in millimeters.
2. Tolerance ±0.10mm (4 mil) unless otherwise specified
3. Package body sizes exclude mold flash and gate burrs. Mold flash at the non-lead sides should be less than 5 mils.
4. Dimension L is measured in gauge plane.
5. Controlling dimension is millimeter, converted inch dimensions are not necessarily exact.