

100V(D-S) N-Channel Enhancement Mode Power MOS FET

General Features

- $V_{DS} = 100V, I_D = 100A$
 $R_{DS(ON)} < 13m\Omega @ V_{GS}=10V$ (Typ:9.9m Ω)
- Special process technology for high ESD capability
- High density cell design for ultra low R_{ds(on)}
- Fully characterized avalanche voltage and current
- Good stability and uniformity with high E_{AS}
- Excellent package for good heat dissipation



Lead Free

Application

- Power switching application
- Hard switched and high frequency circuits
- Uninterruptible power supply

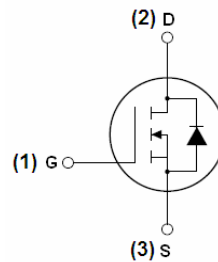


Marking and pin assignment

PIN Configuration



TO-220-3L top view



Schematic diagram

Package Marking and Ordering Information

Device Marking	Device	Device Package	Reel Size	Tape width	Quantity
MSN10B0K	MSN10B0K	TO-220-3L	-	-	-

Absolute Maximum Ratings (T_C=25°C unless otherwise noted)

Symbol	Parameter	Limit	Unit
V _{DS}	Drain-Source Voltage	100	V
V _{GS}	Gate-Source Voltage	±20	V
I _D	Drain Current-Continuous	100	A
I _D (100°C)	Drain Current-Continuous(TC=100°C)	80	A
I _{DM}	Pulsed Drain Current	380	A
P _D	Maximum Power Dissipation	200	W
	Derating factor	1.33	W/°C
E _{AS}	Single pulse avalanche energy ^(Note 5)	800	mJ
T _J , T _{STG}	Operating Junction and Storage Temperature Range	-55 To 175	°C

Thermal Characteristic

$R_{\theta JC}$	Thermal Resistance, Junction-to-Case ^(Note 2)	0.75	$^{\circ}C/W$
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Electrical Characteristics ($T_C=25^{\circ}C$ unless otherwise noted)

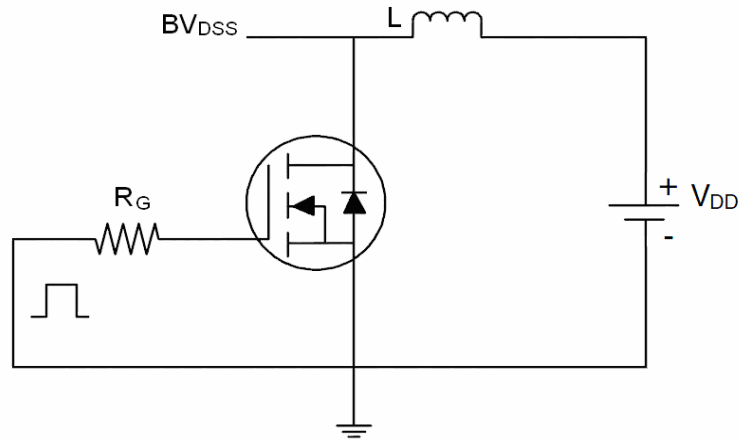
Symbol	Parameter	Condition	Min	Typ	Max	Unit
Off Characteristics						
BV_{DSS}	Drain-Source Breakdown Voltage	$V_{GS}=0V, I_D=250\mu A$	100	110	-	V
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS}=100V, V_{GS}=0V$	-	-	1	μA
I_{GSS}	Gate-Body Leakage Current	$V_{GS}=\pm 20V, V_{DS}=0V$	-	-	± 100	nA
On Characteristics ^(Note 3)						
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS}=V_{GS}, I_D=250\mu A$	2	3	4	V
$R_{DS(ON)}$	Drain-Source On-State Resistance	$V_{GS}=10V, I_D=40A$	-	9.9	13	m Ω
g_{FS}	Forward Transconductance	$V_{DS}=50V, I_D=40A$	100	-	-	S
Dynamic Characteristics ^(Note 4)						
C_{iss}	Input Capacitance	$V_{DS}=50V, V_{GS}=0V,$ $F=1.0MHz$	-	4800	-	PF
C_{oss}	Output Capacitance		-	340	-	PF
C_{riss}	Reverse Transfer Capacitance		-	150	-	PF
Switching Characteristics ^(Note 4)						
$t_{d(on)}$	Turn-on Delay Time	$V_{DD}=50V, I_D=40A$ $V_{GS}=10V, R_{GEN}=2.5\Omega$	-	15	-	nS
t_r	Turn-on Rise Time		-	50	-	nS
$t_{d(off)}$	Turn-Off Delay Time		-	40	-	nS
t_f	Turn-Off Fall Time		-	55	-	nS
Q_g	Total Gate Charge	$V_{DS}=80V, I_D=40A,$ $V_{GS}=10V$	-	85	-	nC
Q_{gs}	Gate-Source Charge		-	18	-	nC
Q_{gd}	Gate-Drain Charge		-	28	-	nC
Drain-Source Diode Characteristics						
V_{SD}	Diode Forward Voltage ^(Note 3)	$V_{GS}=0V, I_S=40A$	-	-	1.2	V
I_S	Diode Forward Current ^(Note 2)	-	-	-	57	A
t_{rr}	Reverse Recovery Time	$T_J = 25^{\circ}C, I_F = 40A$ $di/dt = 100A/\mu s$ (Note3)	-	38	80	nS
Q_{rr}	Reverse Recovery Charge		-	53	100	nC
t_{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by LS+LD)				

Notes:

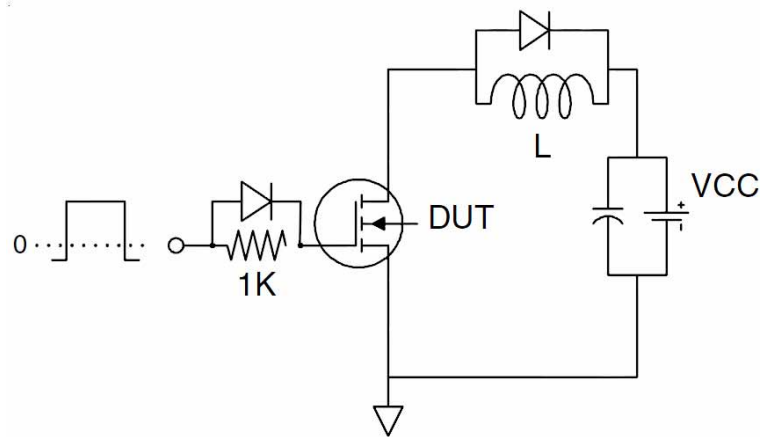
1. Repetitive Rating: Pulse width limited by maximum junction temperature.
2. Surface Mounted on FR4 Board, $t \leq 10$ sec.
3. Pulse Test: Pulse Width $\leq 300\mu s$, Duty Cycle $\leq 2\%$.
4. Guaranteed by design, not subject to production
5. EAS condition: $T_J=25^{\circ}C, V_{DD}=50V, V_G=10V, L=0.5mH, R_g=25\Omega$

Test Circuit

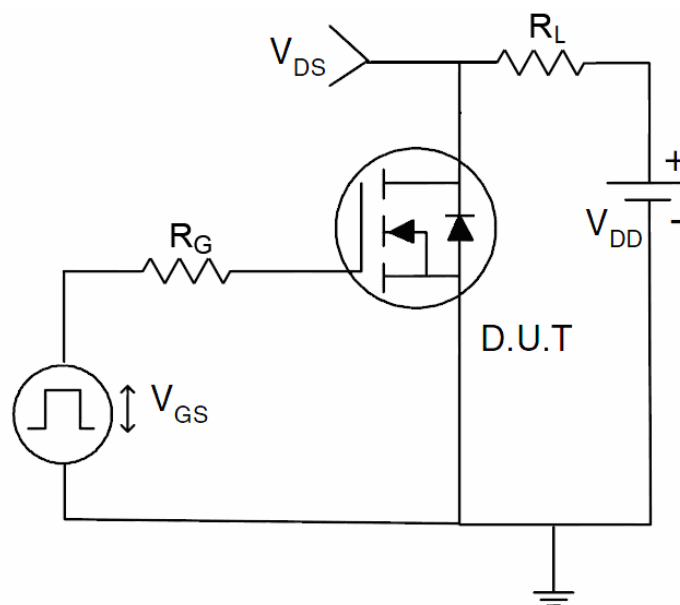
1) E_{AS} test Circuit



2) Gate charge test Circuit



3) Switch Time Test Circuit



Typical Electrical and Thermal Characteristics (Curves)

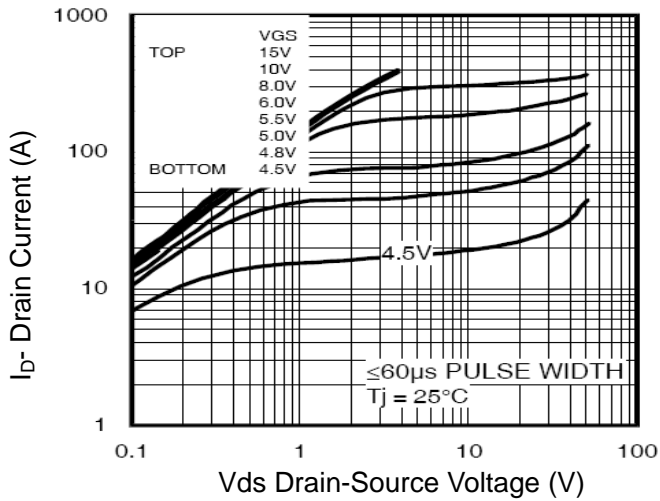


Figure 1 Output Characteristics

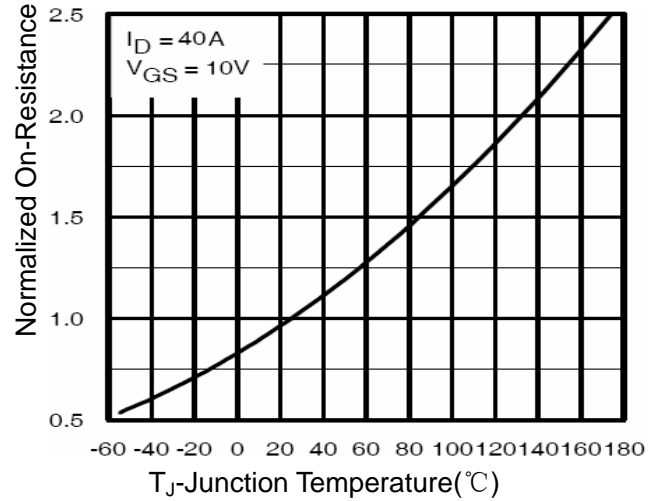


Figure 4 Rdson-Junction Temperature

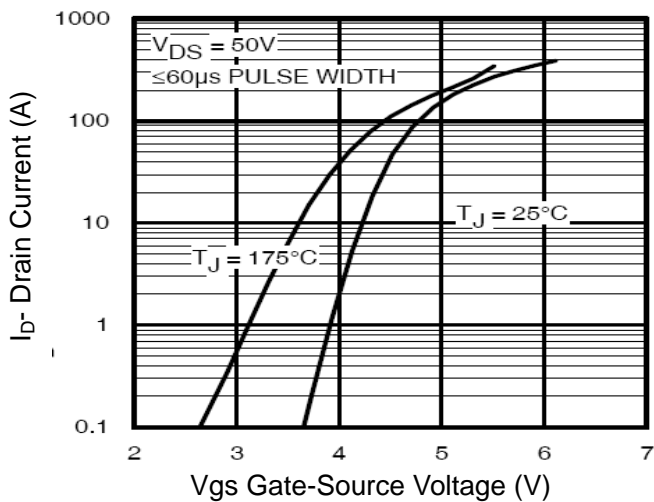


Figure 2 Transfer Characteristics

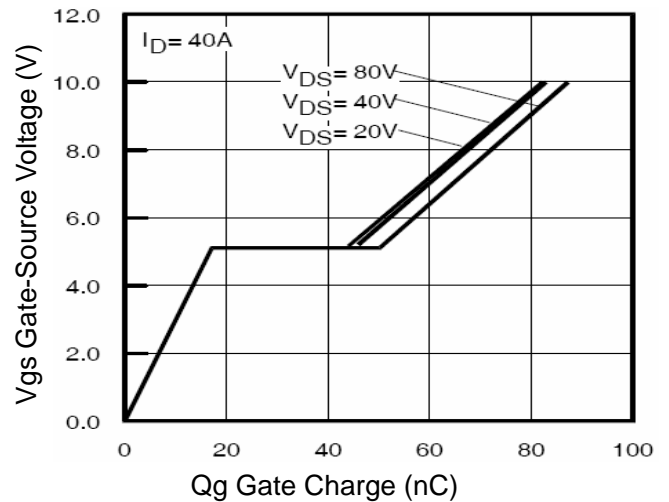


Figure 5 Gate Charge

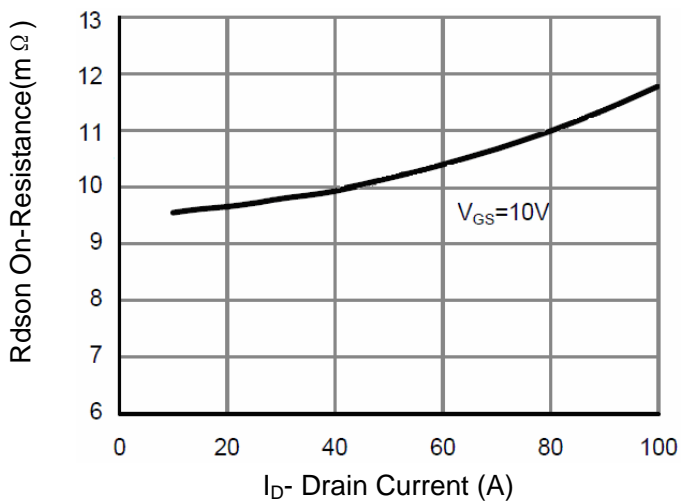


Figure 3 Rdson- Drain Current

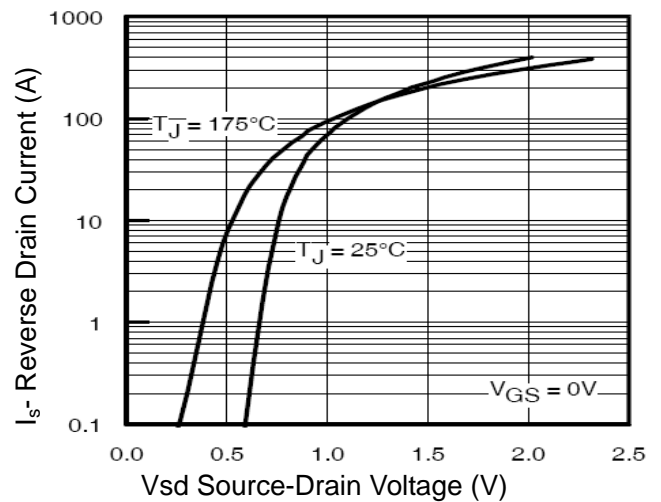


Figure 6 Source- Drain Diode Forward

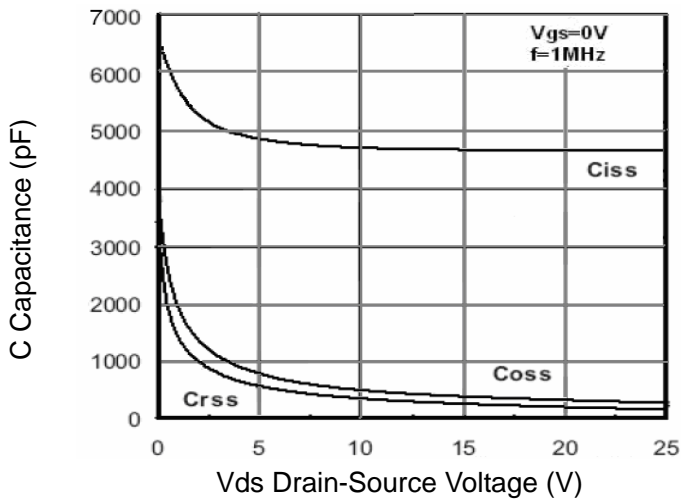


Figure 7 Capacitance vs Vds

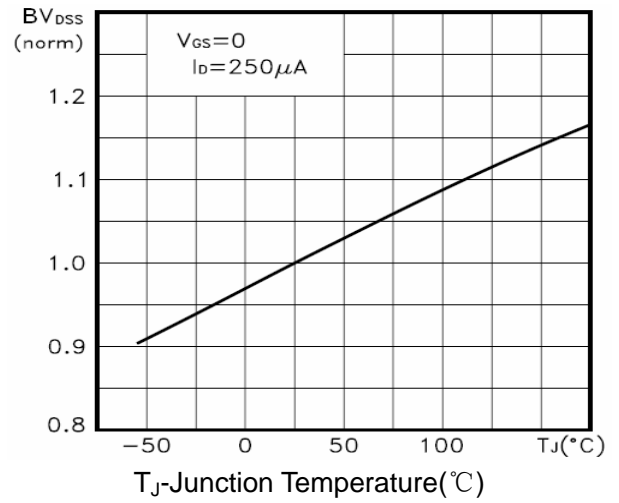


Figure 9 BV_{DSS} vs Junction Temperature

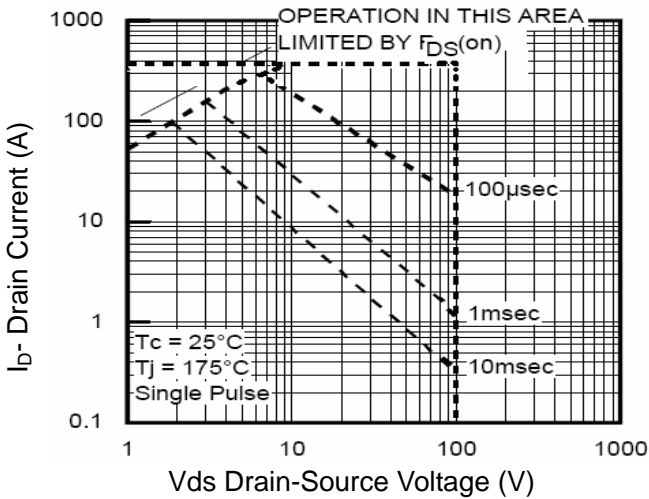


Figure 8 Safe Operation Area

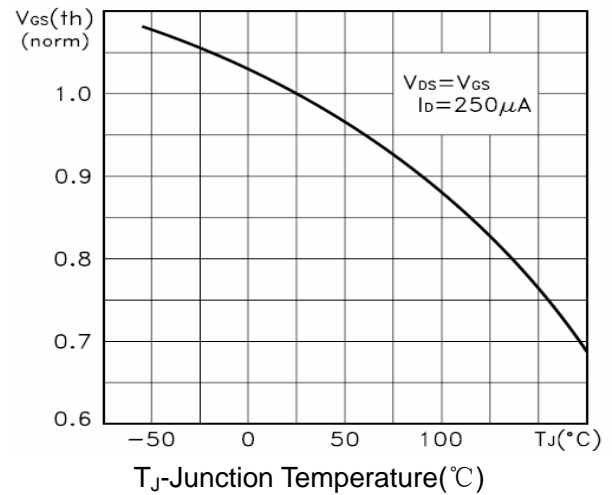


Figure 10 $V_{GS(th)}$ vs Junction Temperature

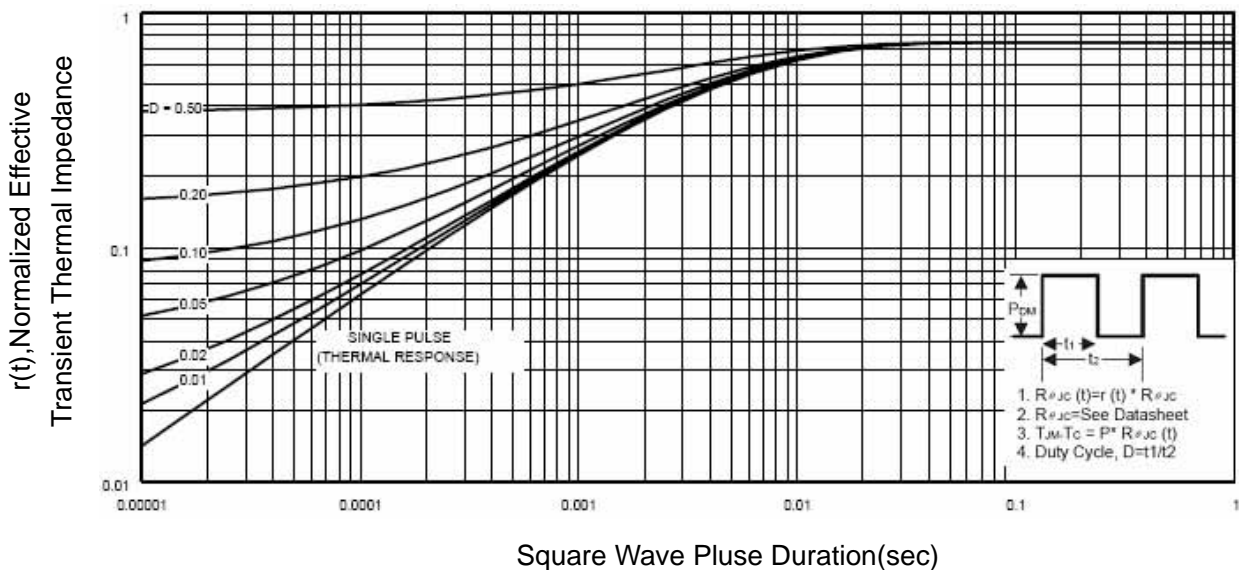
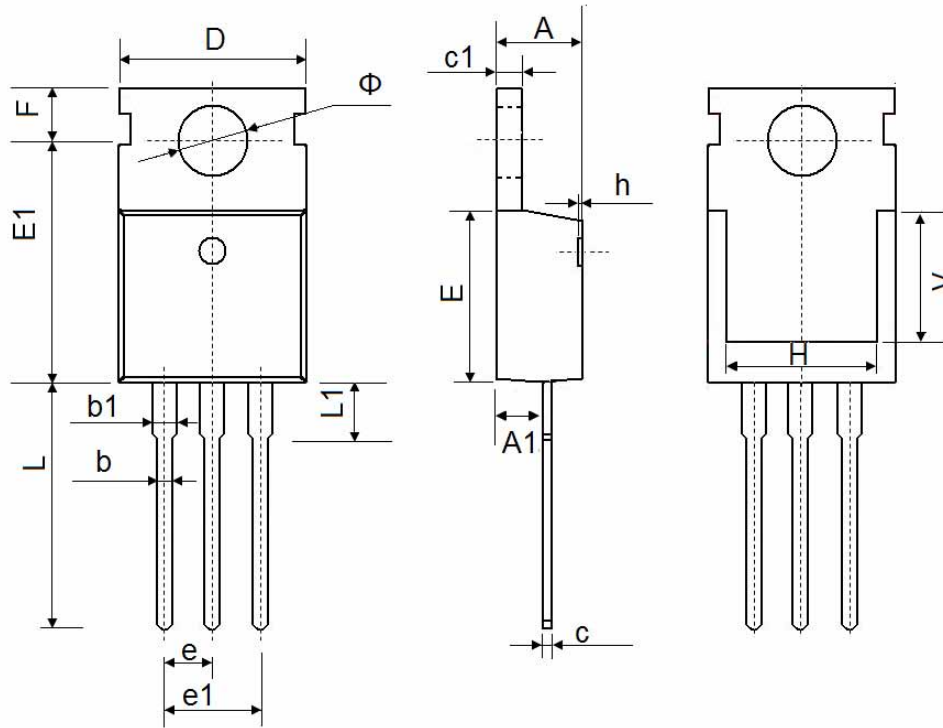


Figure 11 Normalized Maximum Transient Thermal Impedance

TO-220-3L Package Information



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	4.400	4.600	0.173	0.181
A1	2.250	2.550	0.089	0.100
b	0.710	0.910	0.028	0.036
b1	1.170	1.370	0.046	0.054
c	0.330	0.650	0.013	0.026
c1	1.200	1.400	0.047	0.055
D	9.910	10.250	0.390	0.404
E	8.9500	9.750	0.352	0.384
E1	12.650	12.950	0.498	0.510
e	2.540 TYP.		0.100 TYP.	
e1	4.980	5.180	0.196	0.204
F	2.650	2.950	0.104	0.116
H	7.900	8.100	0.311	0.319
h	0.000	0.300	0.000	0.012
L	12.900	13.400	0.508	0.528
L1	2.850	3.250	0.112	0.128
V	7.500 REF.		0.295 REF.	
Φ	3.400	3.800	0.134	0.150