

100V(D-S) N-Channel Enhancement Mode Power MOS FET

General Features

- $V_{DS} = 100V, I_D = 2A$
 $R_{DS(ON)} < 240m\Omega @ V_{GS}=10V$ (Typ:200m Ω)
- High density cell design for ultra low R_{dson}
- Fully characterized avalanche voltage and current
- Excellent package for good heat dissipation



Lead Free

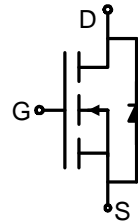
Application

- Power switching application
- Hard switched and high frequency circuits
- Uninterruptible power supply

PIN Configuration



TO-92 view



Schematic diagram

Package Marking and Ordering Information

| Device Marking | Device | Device Package | Reel Size | Tape width | Quantity |
|----------------|----------|----------------|-----------|------------|----------|
| | MSN1006T | TO-92 | - | - | - |

Absolute Maximum Ratings ($T_A=25^\circ C$ unless otherwise noted)

| Parameter | Symbol | Limit | Unit |
|--|----------------|------------|------------|
| Drain-Source Voltage | V_{DS} | 100 | V |
| Gate-Source Voltage | V_{GS} | ± 20 | V |
| Drain Current-Continuous | I_D | 2 | A |
| Drain Current-Pulsed ^(Note 1) | I_{DM} | 5 | A |
| Maximum Power Dissipation | P_D | 1.25 | W |
| Operating Junction and Storage Temperature Range | T_J, T_{STG} | -55 To 150 | $^\circ C$ |

Thermal Characteristic

| | | | |
|---|-----------------|-----|--------------|
| Thermal Resistance, Junction-to-Ambient ^(Note 2) | $R_{\theta JA}$ | 100 | $^\circ C/W$ |
|---|-----------------|-----|--------------|

Electrical Characteristics ($T_A=25^{\circ}\text{C}$ unless otherwise noted)

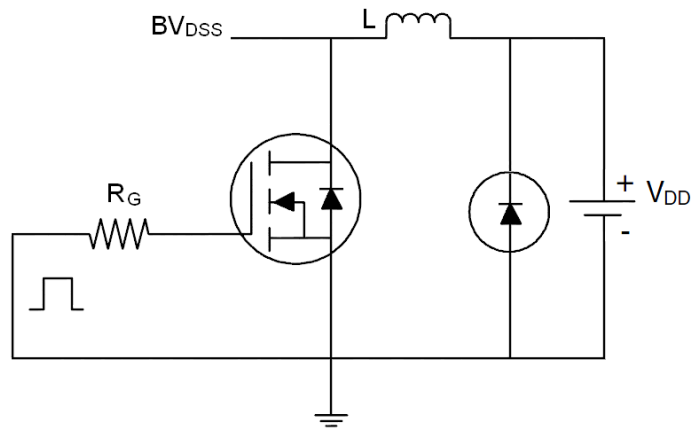
| Parameter | Symbol | Condition | Min | Typ | Max | Unit |
|---|--------------|---|-----|------|-----------|------------|
| Off Characteristics | | | | | | |
| Drain-Source Breakdown Voltage | BV_{DSS} | $V_{GS}=0V, I_D=250\mu A$ | 100 | 110 | - | V |
| Zero Gate Voltage Drain Current | I_{DSS} | $V_{DS}=100V, V_{GS}=0V$ | - | - | 1 | μA |
| Gate-Body Leakage Current | I_{GSS} | $V_{GS}=\pm 20V, V_{DS}=0V$ | - | - | ± 100 | nA |
| On Characteristics (Note 3) | | | | | | |
| Gate Threshold Voltage | $V_{GS(th)}$ | $V_{DS}=V_{GS}, I_D=250\mu A$ | 1.2 | 1.8 | 2.5 | V |
| Drain-Source On-State Resistance | $R_{DS(ON)}$ | $V_{GS}=10V, I_D=1A$ | - | 200 | 240 | m Ω |
| Forward Transconductance | g_{FS} | $V_{DS}=5V, I_D=1A$ | 1 | - | - | S |
| Dynamic Characteristics (Note 4) | | | | | | |
| Input Capacitance | C_{iss} | $V_{DS}=50V, V_{GS}=0V,$ $F=1.0MHz$ | - | 190 | - | PF |
| Output Capacitance | C_{oss} | | - | 22 | - | PF |
| Reverse Transfer Capacitance | C_{rss} | | - | 13 | - | PF |
| Switching Characteristics (Note 4) | | | | | | |
| Turn-on Delay Time | $t_{d(on)}$ | $V_{DD}=50V, I_D=1.3A, R_L=39\Omega$ $V_{GS}=10V, R_G=1\Omega$ | - | 6 | - | nS |
| Turn-on Rise Time | t_r | | - | 10 | - | nS |
| Turn-Off Delay Time | $t_{d(off)}$ | | - | 10 | - | nS |
| Turn-Off Fall Time | t_f | | - | 6 | - | nS |
| Total Gate Charge | Q_g | $V_{DS}=50V, I_D=1.3A,$ $V_{GS}=10V$ | - | 5.2 | - | nC |
| Gate-Source Charge | Q_{gs} | | - | 0.75 | - | nC |
| Gate-Drain Charge | Q_{gd} | | - | 1.4 | - | nC |
| Drain-Source Diode Characteristics | | | | | | |
| Diode Forward Voltage (Note 3) | V_{SD} | $V_{GS}=0V, I_S=1.3A$ | - | - | 1.2 | V |
| Diode Forward Current (Note 2) | I_S | | - | - | 2 | A |

Notes:

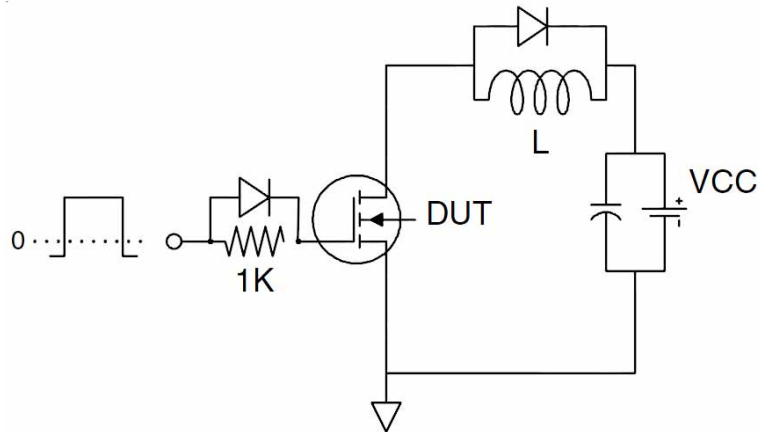
1. Repetitive Rating: Pulse width limited by maximum junction temperature.
2. Surface Mounted on FR4 Board, $t \leq 10$ sec.
3. Pulse Test: Pulse Width $\leq 300\mu s$, Duty Cycle $\leq 2\%$.
4. Guaranteed by design, not subject to production

Test Circuit

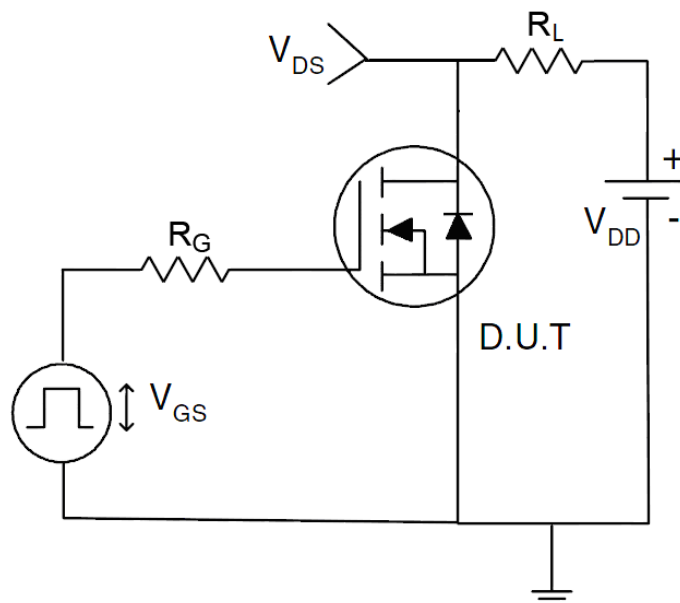
1) E_{AS} test circuit



2) Gate charge test circuit



3) Switch Time Test Circuit



Typical Electrical and Thermal Characteristics (Curves)

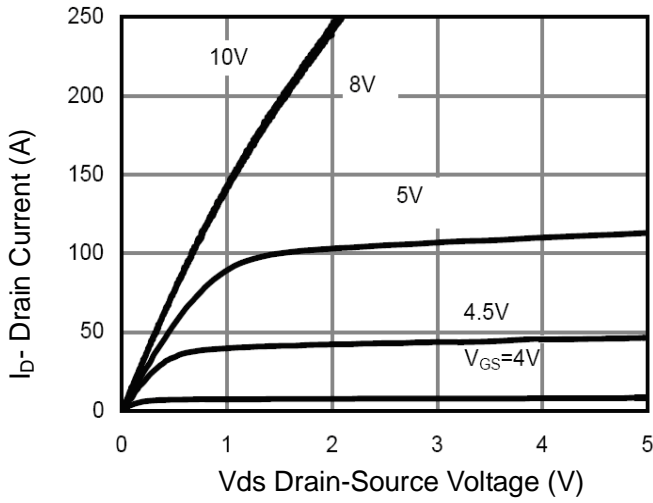


Figure 1 Output Characteristics

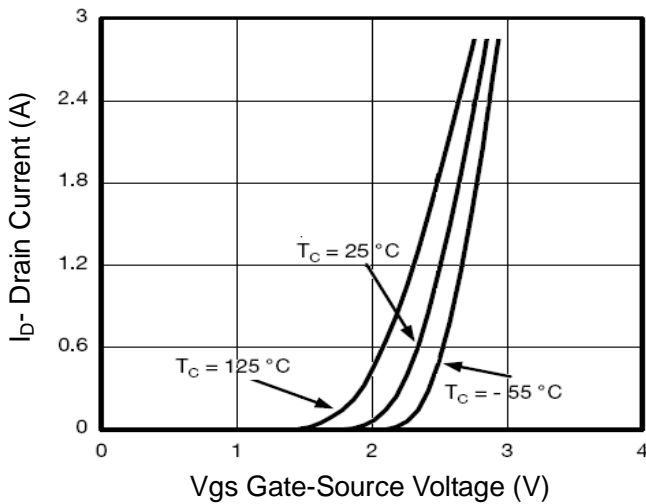


Figure 2 Transfer Characteristics

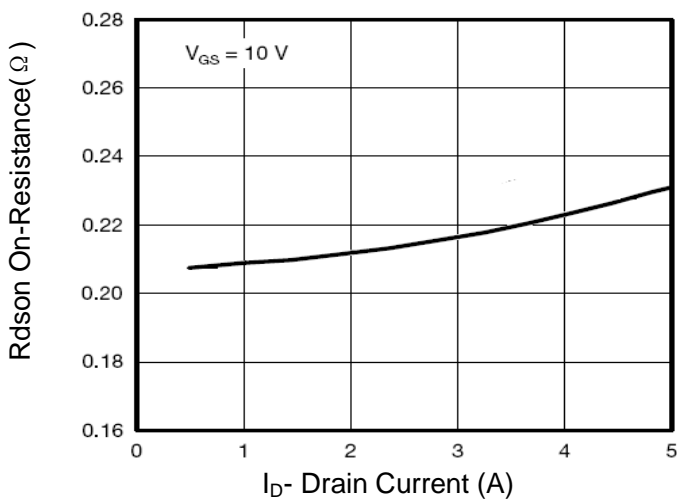


Figure 3 Rdson- Drain Current

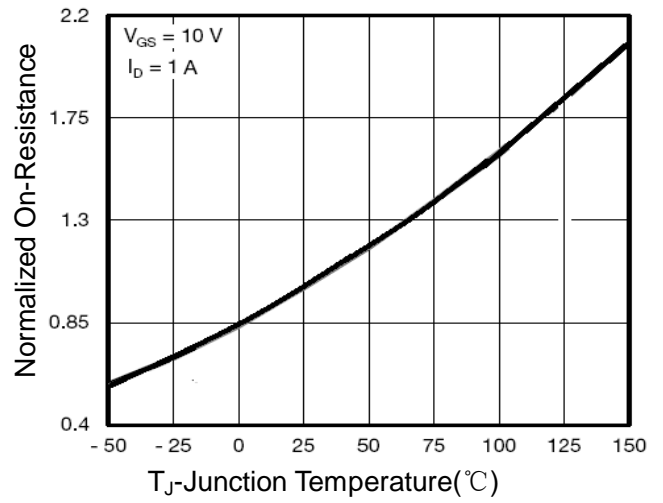


Figure 4 Rdson-Junction Temperature

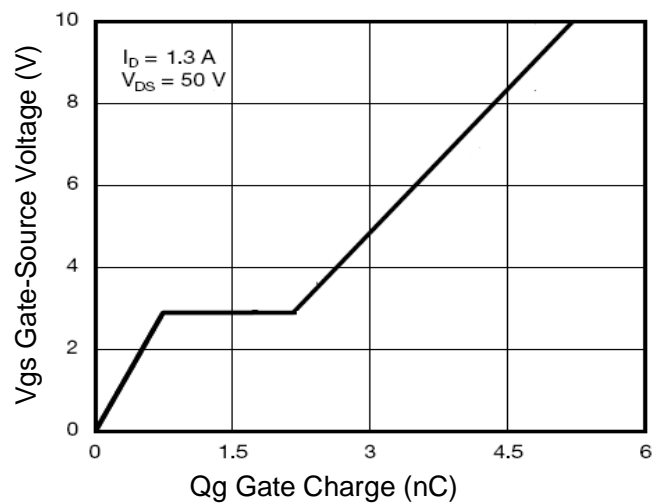


Figure 5 Gate Charge

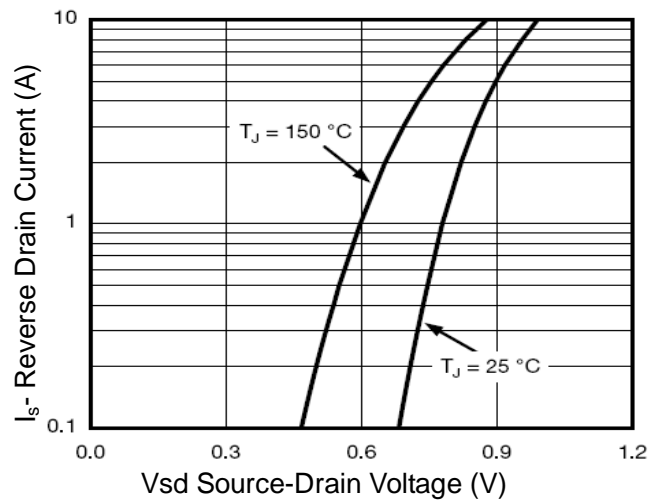


Figure 6 Source- Drain Diode Forward

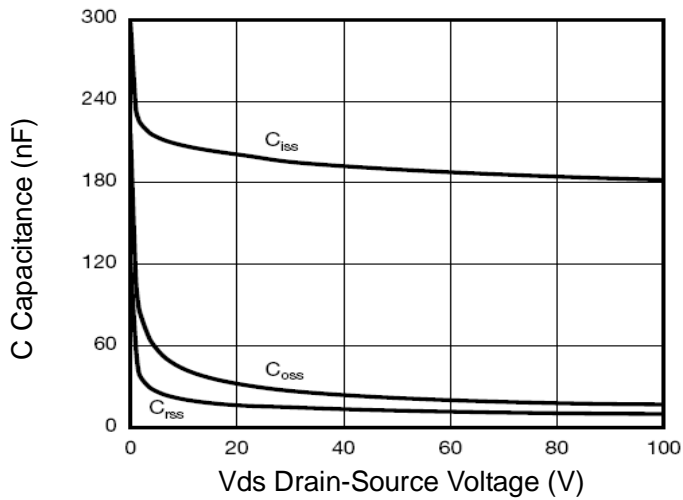


Figure 7 Capacitance vs Vds

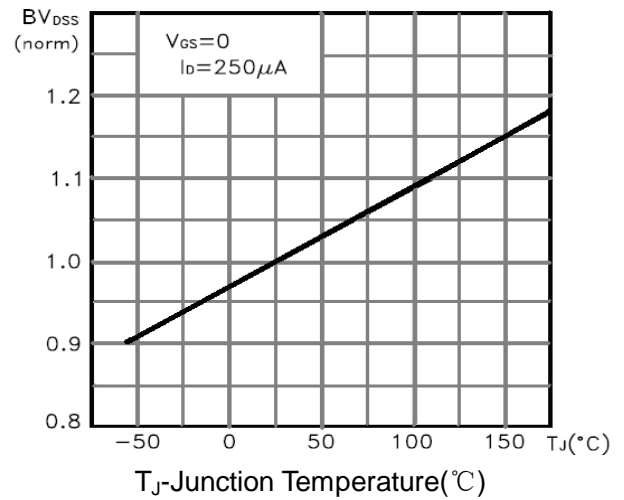


Figure 9 BV_{DSS} vs Junction Temperature

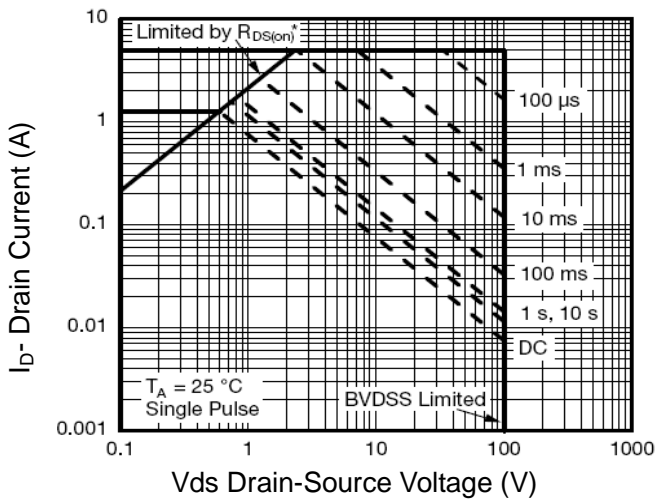


Figure 8 Safe Operation Area

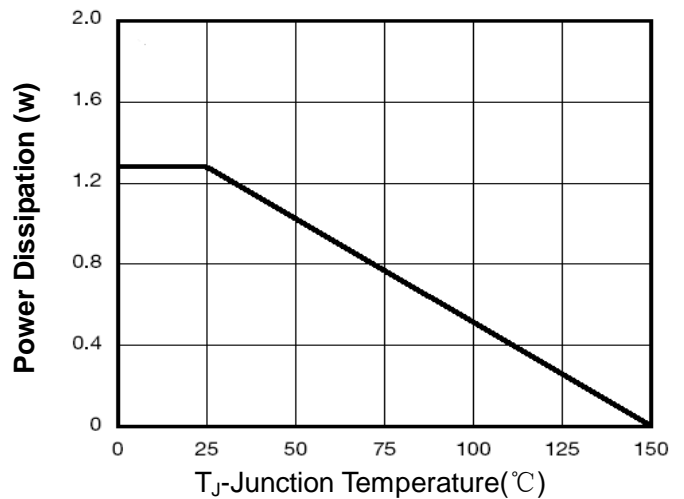


Figure 10 Power De-rating

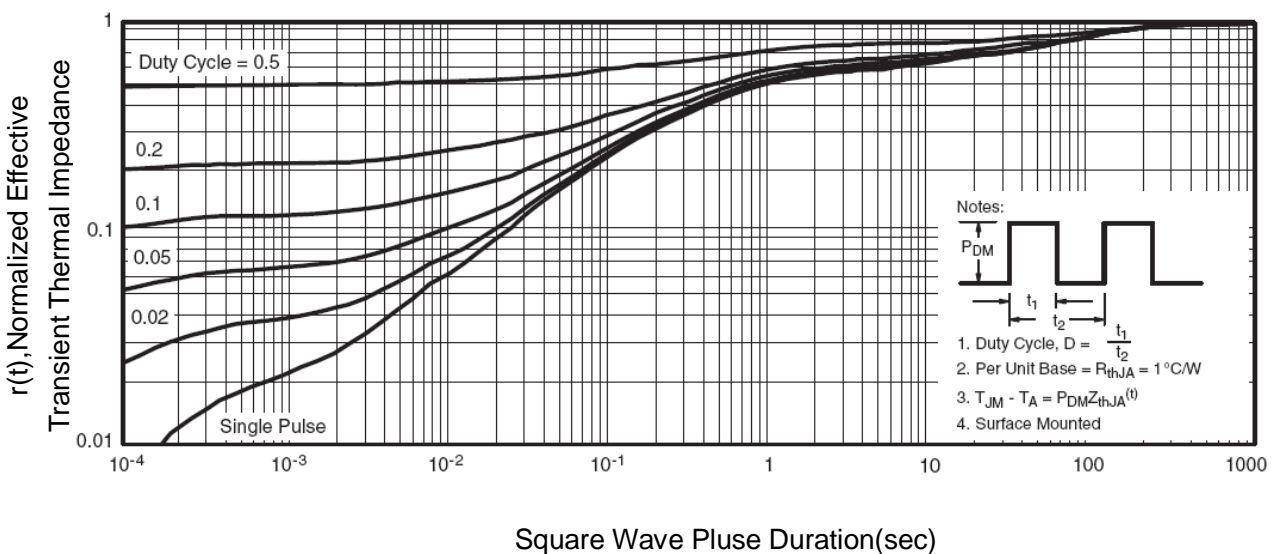
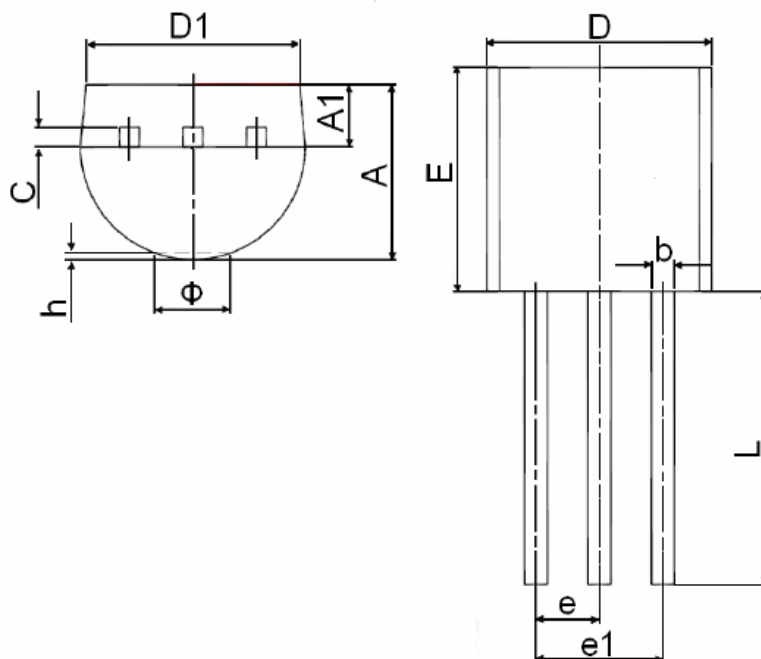


Figure 11 Normalized Maximum Transient Thermal Impedance

TO-92 Package Information



| Symbol | Dimensions In Millimeters | | Dimensions In Inches | |
|--------|---------------------------|--------|----------------------|-------|
| | Min | Max | Min | Max |
| A | 3.300 | 3.700 | 0.130 | 0.146 |
| A1 | 1.100 | 1.400 | 0.043 | 0.055 |
| b | 0.380 | 0.550 | 0.015 | 0.022 |
| c | 0.360 | 0.510 | 0.014 | 0.020 |
| D | 4.400 | 4.700 | 0.173 | 0.185 |
| D1 | 3.430 | | 0.135 | |
| E | 4.300 | 4.700 | 0.169 | 0.185 |
| e | 1.270 TYP | | 0.050 TYP | |
| e1 | 2.440 | 2.640 | 0.096 | 0.104 |
| L | 14.100 | 14.500 | 0.555 | 0.571 |
| Φ | | 1.600 | | 0.063 |
| h | 0.000 | 0.380 | 0.000 | 0.015 |

Notes

1. All dimensions are in millimeters.
2. Tolerance $\pm 0.10\text{mm}$ (4 mil) unless otherwise specified
3. Package body sizes exclude mold flash and gate burrs. Mold flash at the non-lead sides should be less than 5 mils.
4. Dimension L is measured in gauge plane.
5. Controlling dimension is millimeter, converted inch dimensions are not necessarily exact.