

60V(D-S) N-Channel Enhancement Mode Power MOS FET

General Features

- $V_{DS} = 60V, I_D = 150A$
 $R_{DS(ON)} < 4.5m\Omega @ V_{GS} = 10V$
- High density cell design for ultra low R_{dson}
- Fully characterized avalanche voltage and current
- Good stability and uniformity with high E_{AS}
- Excellent package for good heat dissipation
- Special process technology for high ESD capability

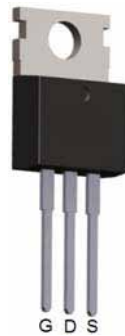


Lead Free

Application

- Power switching application
- Hard switched and high frequency circuits
- Uninterruptible power supply

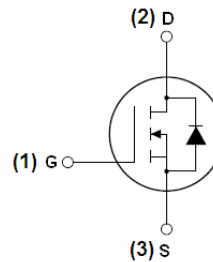
PIN Configuration



TO-220-3L top view



Marking and pin assignment



Schematic diagram

Package Marking and Ordering Information

| Device Marking | Device | Device Package | Reel Size | Tape width | Quantity |
|----------------|----------|----------------|-----------|------------|----------|
| MSN06B5K | MSN06B5K | TO-220-3L | - | - | - |

Absolute Maximum Ratings ($T_C = 25^\circ C$ unless otherwise noted)

| Parameter | Symbol | Limit | Unit |
|---|--------------------|------------|---------------|
| Drain-Source Voltage | V_{DS} | 60 | V |
| Gate-Source Voltage | V_{GS} | ± 20 | V |
| Drain Current-Continuous | I_D | 150 | A |
| Drain Current-Continuous($T_C = 100^\circ C$) | $I_D(100^\circ C)$ | 105 | A |
| Pulsed Drain Current | I_{DM} | 600 | A |
| Maximum Power Dissipation | P_D | 220 | W |
| Derating factor | | 1.47 | W/ $^\circ C$ |
| Single pulse avalanche energy ^(Note 5) | E_{AS} | 1400 | mJ |
| Operating Junction and Storage Temperature Range | T_J, T_{STG} | -55 To 175 | $^\circ C$ |

Thermal Characteristic

| | | | |
|--|-----------------|------|------|
| Thermal Resistance, Junction-to-Case ^(Note 2) | $R_{\theta JC}$ | 0.68 | °C/W |
|--|-----------------|------|------|

Electrical Characteristics ($T_C=25^\circ\text{C}$ unless otherwise noted)

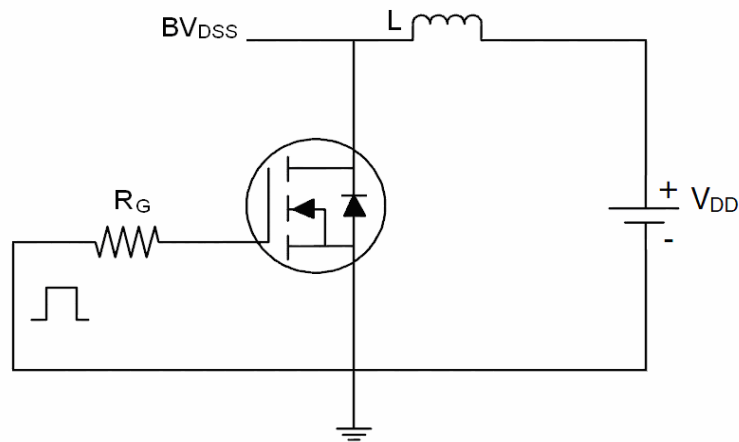
| Parameter | Symbol | Condition | Min | Typ | Max | Unit |
|--|--------------|---|-----|------|-----------|------------|
| Off Characteristics | | | | | | |
| Drain-Source Breakdown Voltage | BV_{DSS} | $V_{GS}=0V, I_D=250\mu A$ | 60 | 68 | - | V |
| Zero Gate Voltage Drain Current | I_{DSS} | $V_{DS}=60V, V_{GS}=0V$ | - | - | 1 | μA |
| Gate-Body Leakage Current | I_{GSS} | $V_{GS}=\pm 20V, V_{DS}=0V$ | - | - | ± 100 | nA |
| On Characteristics ^(Note 3) | | | | | | |
| Gate Threshold Voltage | $V_{GS(th)}$ | $V_{DS}=V_{GS}, I_D=250\mu A$ | 2 | 3 | 4 | V |
| Drain-Source On-State Resistance | $R_{DS(on)}$ | $V_{GS}=10V, I_D=75A$ | - | 3.4 | 4.5 | m Ω |
| Forward Transconductance | g_{FS} | $V_{DS}=50V, I_D=75A$ | 180 | - | - | S |
| Dynamic Characteristics ^(Note 4) | | | | | | |
| Input Capacitance | C_{iss} | $V_{DS}=25V, V_{GS}=0V,$ $F=1.0\text{MHz}$ | - | 6500 | - | PF |
| Output Capacitance | C_{oss} | | - | 650 | - | PF |
| Reverse Transfer Capacitance | C_{rss} | | - | 590 | - | PF |
| Switching Characteristics ^(Note 4) | | | | | | |
| Turn-on Delay Time | $t_{d(on)}$ | $V_{DD}=30V, I_D=2A, R_L=15\Omega$ $V_{GS}=10V, R_G=2.5\Omega$ | - | 26 | - | nS |
| Turn-on Rise Time | t_r | | - | 24 | - | nS |
| Turn-Off Delay Time | $t_{d(off)}$ | | - | 91 | - | nS |
| Turn-Off Fall Time | t_f | | - | 39 | - | nS |
| Total Gate Charge | Q_g | $V_{DS}=30V, I_D=30A,$ $V_{GS}=10V$ | - | 163 | - | nC |
| Gate-Source Charge | Q_{gs} | | - | 31 | - | nC |
| Gate-Drain Charge | Q_{gd} | | - | 64 | - | nC |
| Drain-Source Diode Characteristics | | | | | | |
| Diode Forward Voltage ^(Note 3) | V_{SD} | $V_{GS}=0V, I_S=40A$ | - | - | 1.2 | V |
| Diode Forward Current ^(Note 2) | I_S | | - | - | 150 | A |
| Reverse Recovery Time | t_{rr} | $T_J = 25^\circ\text{C}, I_F = 40A$ $di/dt = 100A/\mu\text{s}$ ^(Note 3) | - | 42 | 60 | nS |
| Reverse Recovery Charge | Q_{rr} | | - | 66 | 80 | nC |
| Forward Turn-On Time | t_{on} | Intrinsic turn-on time is negligible (turn-on is dominated by LS+LD) | | | | |

Notes:

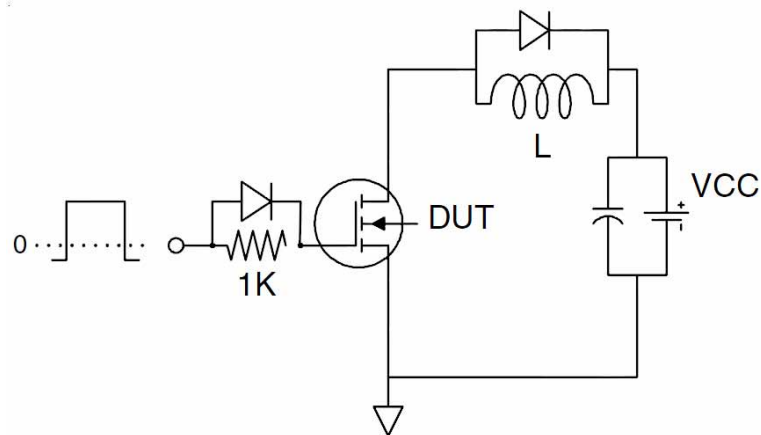
1. Repetitive Rating: Pulse width limited by maximum junction temperature.
2. Surface Mounted on FR4 Board, $t \leq 10$ sec.
3. Pulse Test: Pulse Width $\leq 300\mu\text{s}$, Duty Cycle $\leq 2\%$.
4. Guaranteed by design, not subject to production
5. EAS condition: $T_J=25^\circ\text{C}, V_{DD}=30V, V_G=10V, L=0.5\text{mH}, R_G=25\Omega$

Test circuit

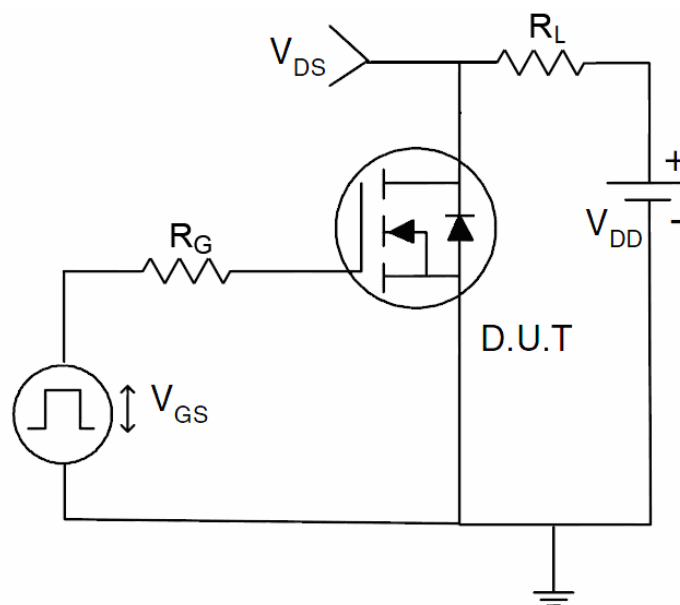
1) E_{AS} test Circuits



2) Gate charge test Circuit:



3) Switch Time Test Circuit:



Typical Electrical and Thermal Characteristics (Curves)

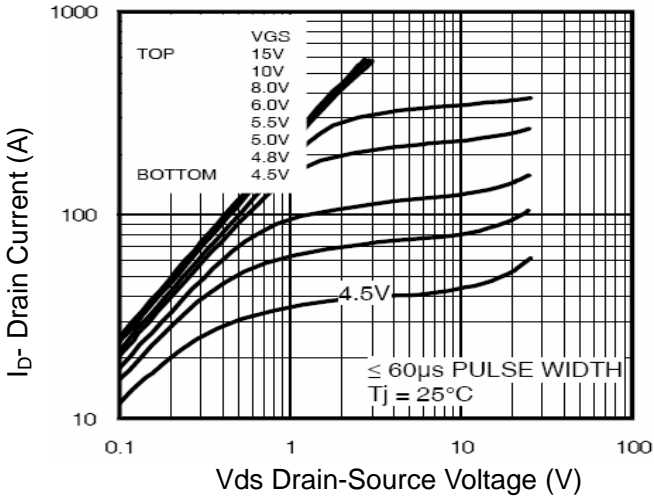


Figure 1 Output Characteristics

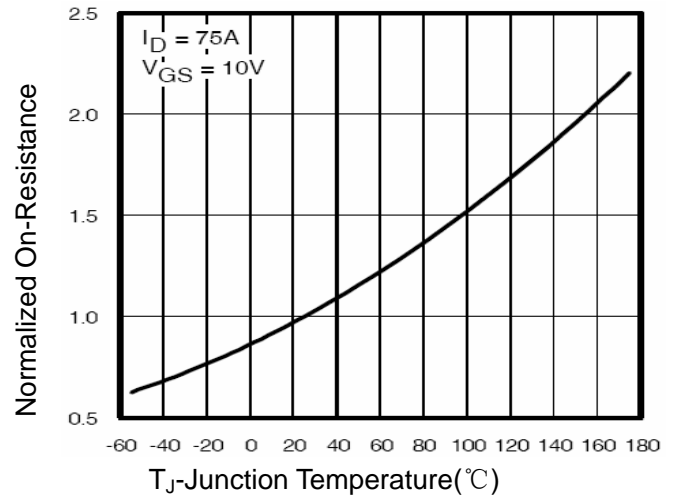


Figure 4 R_{dson} -Junction Temperature

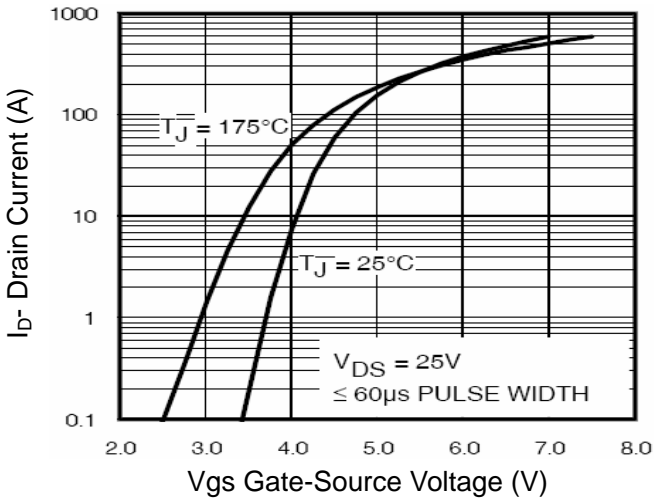


Figure 2 Transfer Characteristics

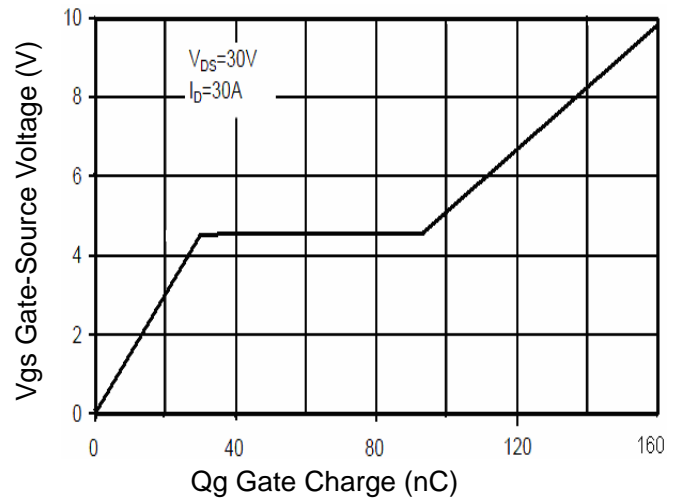


Figure 5 Gate Charge

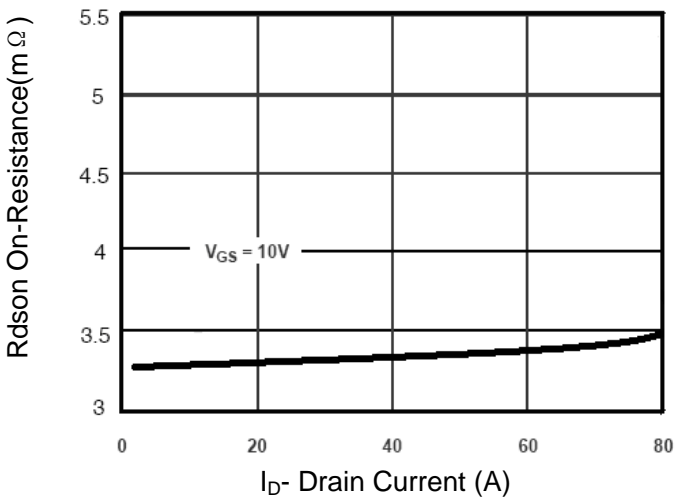


Figure 3 R_{dson} - Drain Current

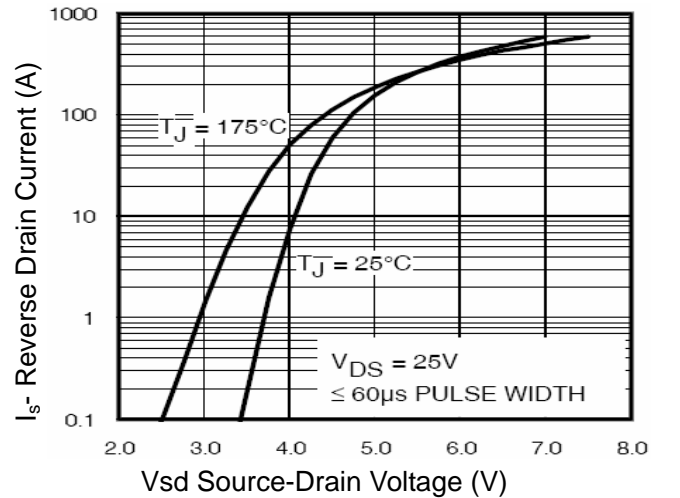


Figure 6 Source- Drain Diode Forward

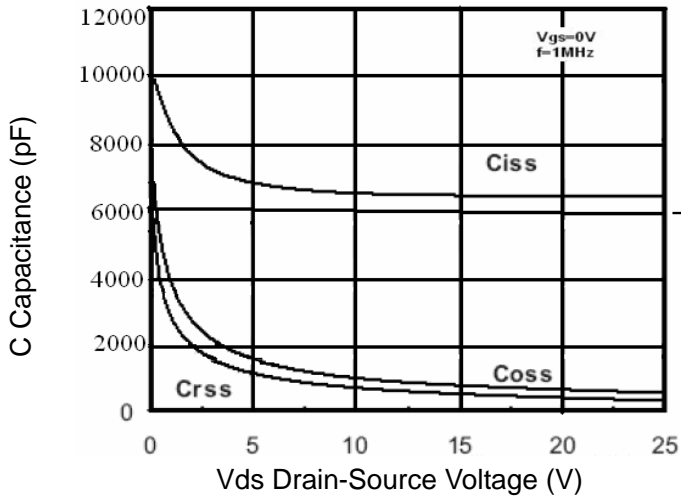


Figure 7 Capacitance vs Vds

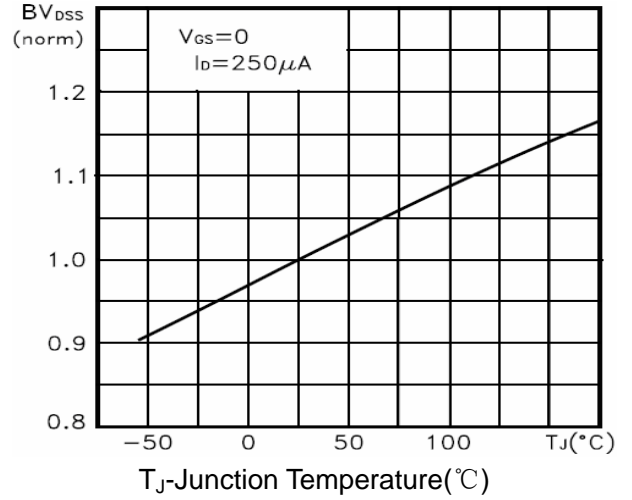


Figure 9 BV_{DSS} vs Junction Temperature

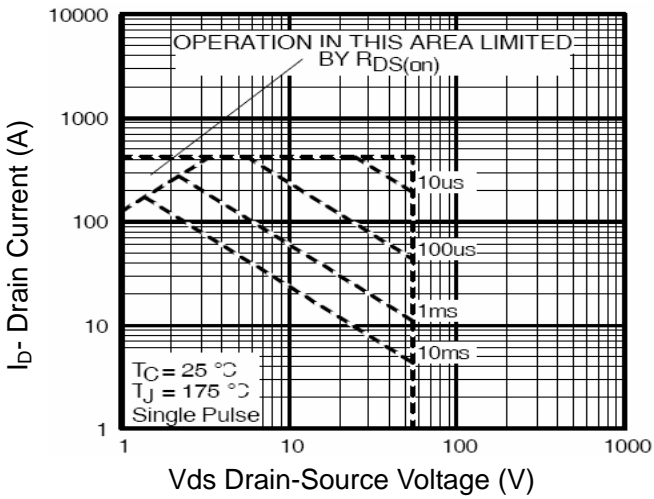


Figure 8 Safe Operation Area

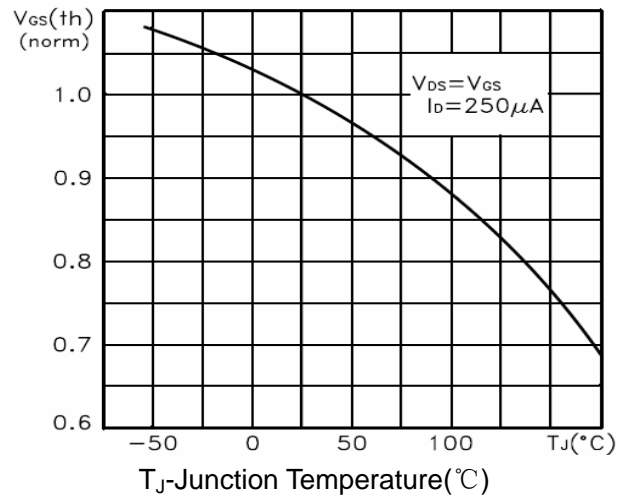


Figure 10 $V_{GS(th)}$ vs Junction Temperature

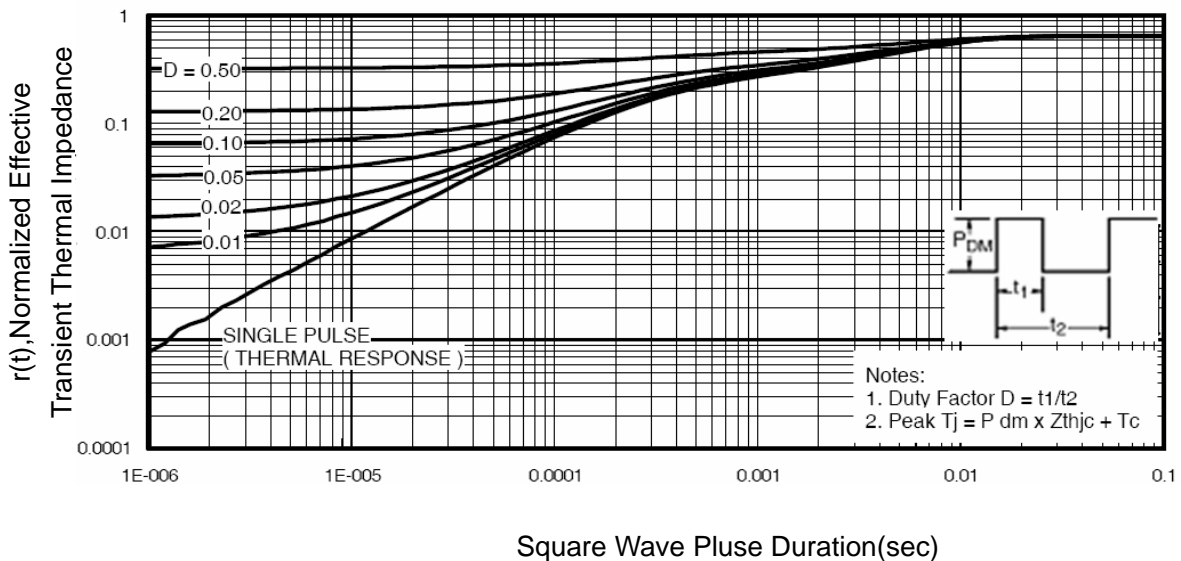
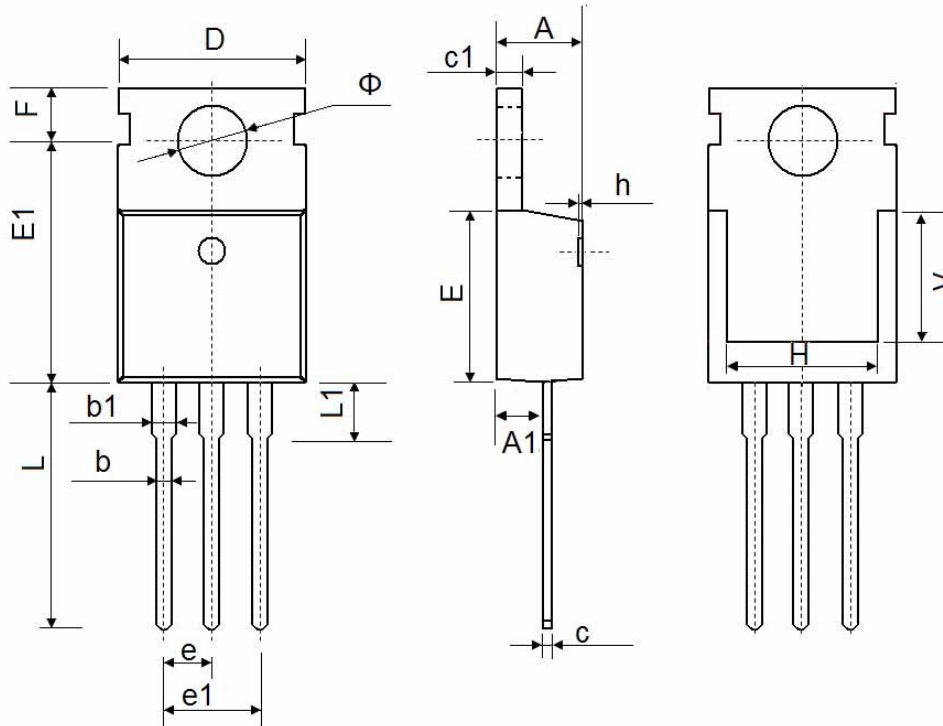


Figure 11 Normalized Maximum Transient Thermal Impedance

TO-220-3L Package Information



| Symbol | Dimensions In Millimeters | | Dimensions In Inches | |
|--------|---------------------------|--------|----------------------|-------|
| | Min. | Max. | Min. | Max. |
| A | 4.400 | 4.600 | 0.173 | 0.181 |
| A1 | 2.250 | 2.550 | 0.089 | 0.100 |
| b | 0.710 | 0.910 | 0.028 | 0.036 |
| b1 | 1.170 | 1.370 | 0.046 | 0.054 |
| c | 0.330 | 0.650 | 0.013 | 0.026 |
| c1 | 1.200 | 1.400 | 0.047 | 0.055 |
| D | 9.910 | 10.250 | 0.390 | 0.404 |
| E | 8.9500 | 9.750 | 0.352 | 0.384 |
| E1 | 12.650 | 12.950 | 0.498 | 0.510 |
| e | 2.540 TYP. | | 0.100 TYP. | |
| e1 | 4.980 | 5.180 | 0.196 | 0.204 |
| F | 2.650 | 2.950 | 0.104 | 0.116 |
| H | 7.900 | 8.100 | 0.311 | 0.319 |
| h | 0.000 | 0.300 | 0.000 | 0.012 |
| L | 12.900 | 13.400 | 0.508 | 0.528 |
| L1 | 2.850 | 3.250 | 0.112 | 0.128 |
| V | 7.500 REF. | | 0.295 REF. | |
| Φ | 3.400 | 3.800 | 0.134 | 0.150 |