

30V(D-S) N-Channel Enhancement Mode Power MOS FET

General Features

- $V_{DS} = 30V, I_D = 10A$
 $R_{DS(ON)} < 12m\Omega @ V_{GS}=10V$
 $R_{DS(ON)} < 16m\Omega @ V_{GS}=4.5V$
- High density cell design for ultra low R_{ds(on)}
- Fully characterized Avalanche voltage and current

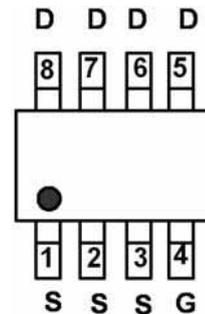


Lead Free

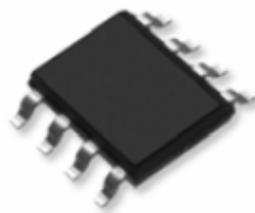
Application

- Power switching application
- Hard Switched and High Frequency Circuits
- Uninterruptible Power Supply

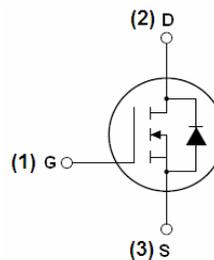
PIN Configuration



Marking and pin assignment



SOP-8 top view



Schematic diagram

Package Marking and Ordering Information

Device Marking	Device	Device Package	Reel Size	Tape width	Quantity
MSN0310W	MSN0310W	SOP-8	Ø330mm	12mm	2500 units

Absolute Maximum Ratings (T_A=25°C unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V _{DS}	30	V
Gate-Source Voltage	V _{GS}	±20	V
Drain Current-Continuous	I _D	10	A
Drain Current-Continuous(T _C =100°C)	I _D (100°C)	6	A
Pulsed Drain Current	I _{DM}	50	A
Maximum Power Dissipation	P _D	2.5	W
Operating Junction and Storage Temperature Range	T _J , T _{STG}	-55 To 150	°C

Thermal Characteristic

Thermal Resistance, Junction-to-Case ^(Note 2)	R _{θJC}	50	°C/W
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Electrical Characteristics ($T_A=25^{\circ}\text{C}$ unless otherwise noted)

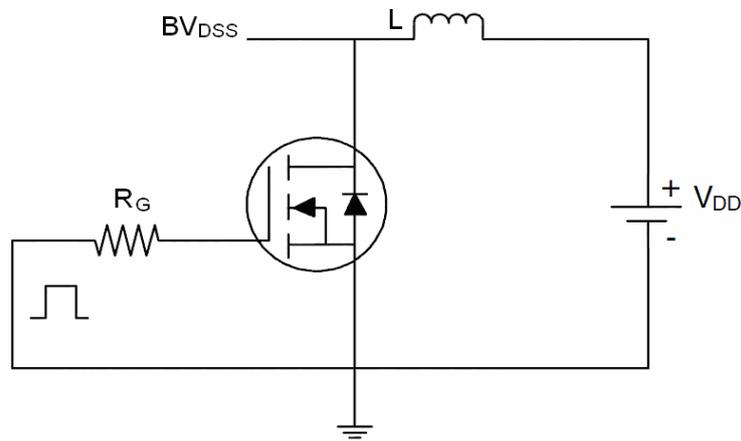
Parameter	Symbol	Condition	Min	Typ	Max	Unit
Off Characteristics						
Drain-Source Breakdown Voltage	BV_{DSS}	$V_{GS}=0V, I_D=250\mu A$	30	33	-	V
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS}=30V, V_{GS}=0V$	-	-	1	μA
Gate-Body Leakage Current	I_{GSS}	$V_{GS}=\pm 20V, V_{DS}=0V$	-	-	± 100	nA
On Characteristics (Note 3)						
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=250\mu A$	1	1.6	3	V
Drain-Source On-State Resistance	$R_{DS(on)}$	$V_{GS}=10V, I_D=10A$	-	8	12	m Ω
		$V_{GS}=4.5V, I_D=5A$	-	11	16	
Forward Transconductance	g_{FS}	$V_{DS}=5V, I_D=10A$	15	-	-	S
Dynamic Characteristics (Note 4)						
Input Capacitance	C_{iss}	$V_{DS}=15V, V_{GS}=0V,$ $F=1.0MHz$	-	1550	-	PF
Output Capacitance	C_{oss}		-	300	-	PF
Reverse Transfer Capacitance	C_{rss}		-	180	-	PF
Switching Characteristics (Note 4)						
Turn-on Delay Time	$t_{d(on)}$	$V_{DD}=25V, I_D=1A$ $V_{GS}=10V, R_{GEN}=6\Omega$	-	30	-	nS
Turn-on Rise Time	t_r		-	20	-	nS
Turn-Off Delay Time	$t_{d(off)}$		-	100	-	nS
Turn-Off Fall Time	t_f		-	80	-	nS
Total Gate Charge	Q_g	$V_{DS}=15V, I_D=10A,$ $V_{GS}=5V$	-	13	-	nC
Gate-Source Charge	Q_{gs}		-	5.5	-	nC
Gate-Drain Charge	Q_{gd}		-	3.5	-	nC
Drain-Source Diode Characteristics						
Diode Forward Voltage (Note 3)	V_{SD}	$V_{GS}=0V, I_S=10A$	-	-	1.2	V
Diode Forward Current (Note 2)	I_S		-	-	10	A

Notes:

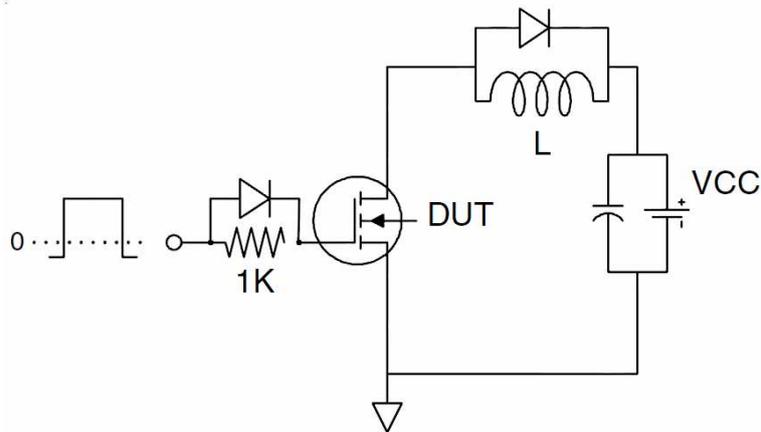
1. Repetitive Rating: Pulse width limited by maximum junction temperature.
2. Surface Mounted on FR4 Board, $t \leq 10$ sec.
3. Pulse Test: Pulse Width $\leq 300\mu s$, Duty Cycle $\leq 2\%$.
4. Guaranteed by design, not subject to production

Test Circuit

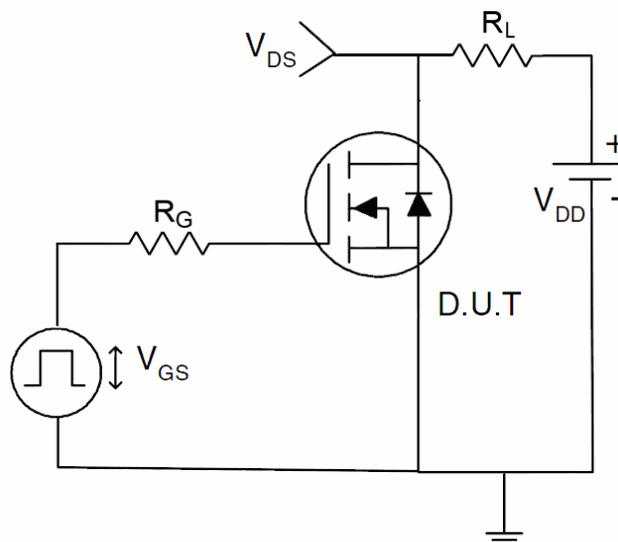
1) E_{AS} Test Circuits



2) Gate Charge Test Circuit:



3) Switch Time Test Circuit:



Typical Electrical and Thermal Characteristics (Curves)

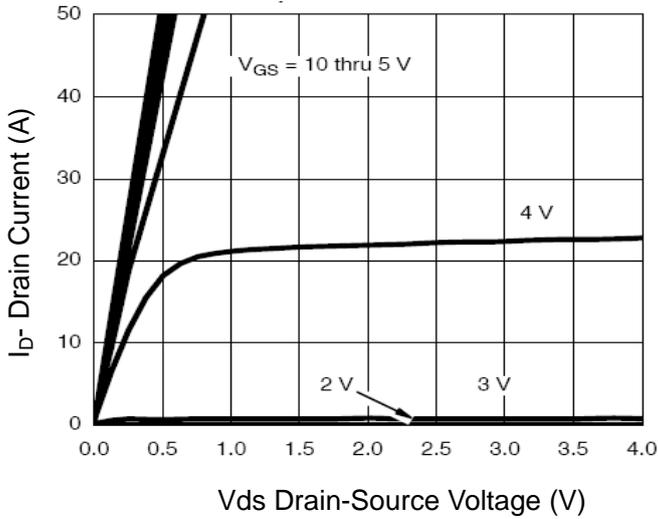


Figure 1 Output Characteristics

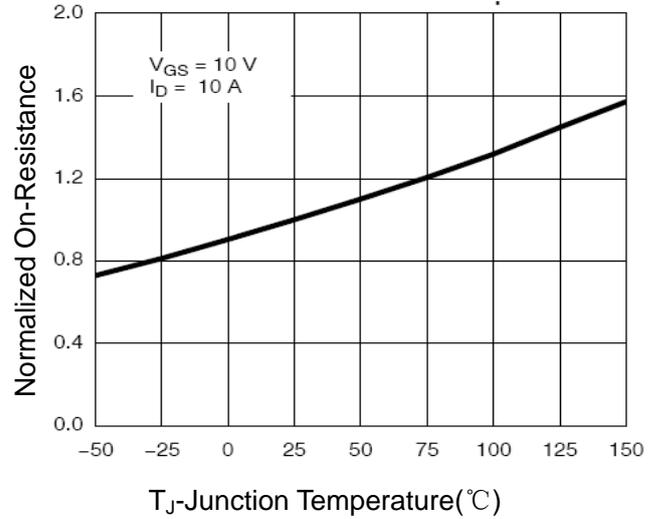


Figure 4 R_{dson} -Junction Temperature

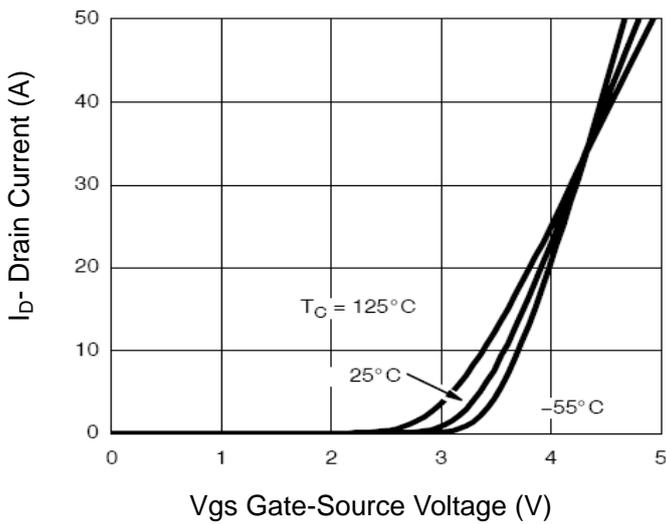


Figure 2 Transfer Characteristics

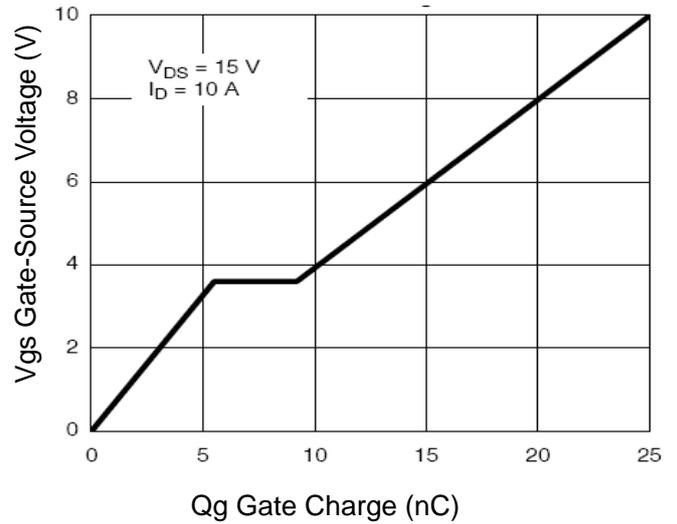


Figure 5 Gate Charge

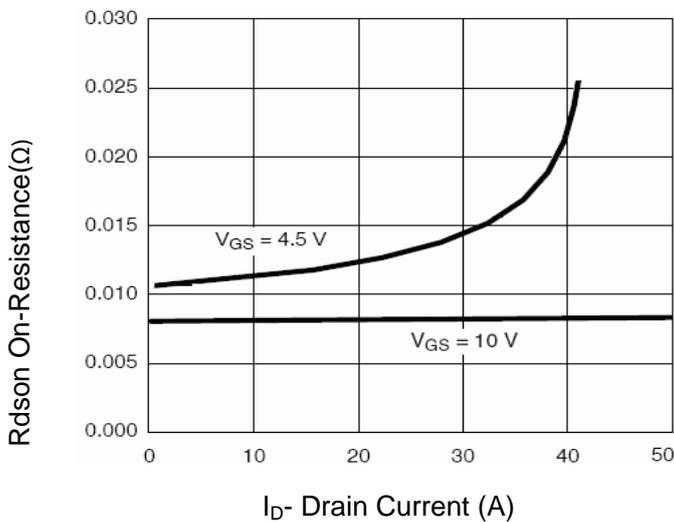


Figure 3 R_{dson} - Drain Current

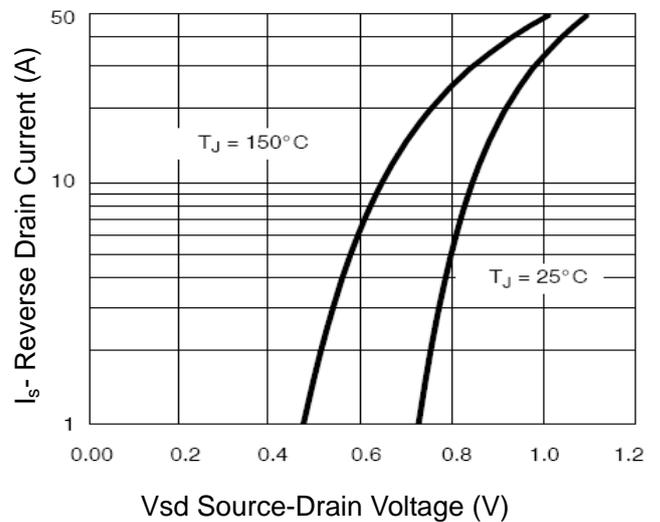


Figure 6 Source- Drain Diode Forward

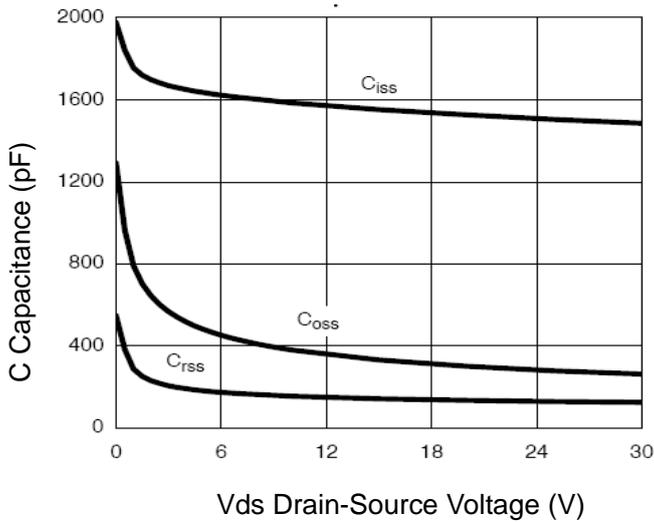


Figure 7 Capacitance vs Vds

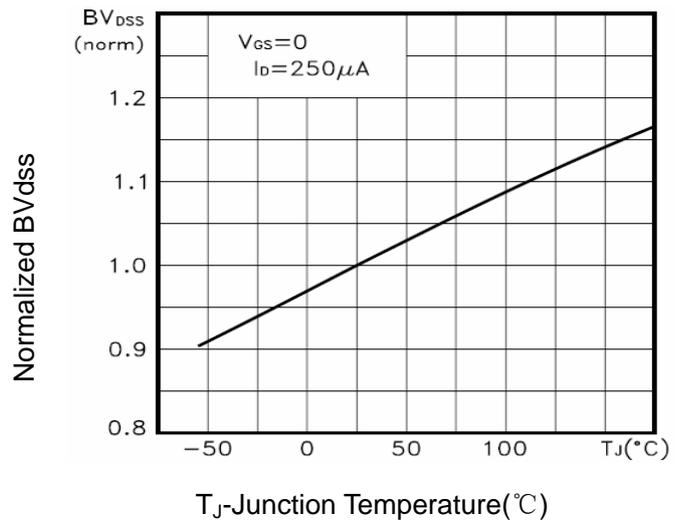


Figure 9 BV_{DSS} vs Junction Temperature

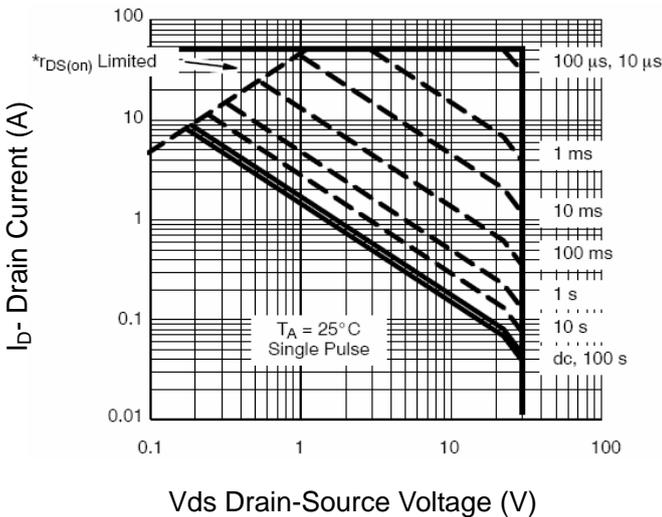


Figure 8 Safe Operation Area

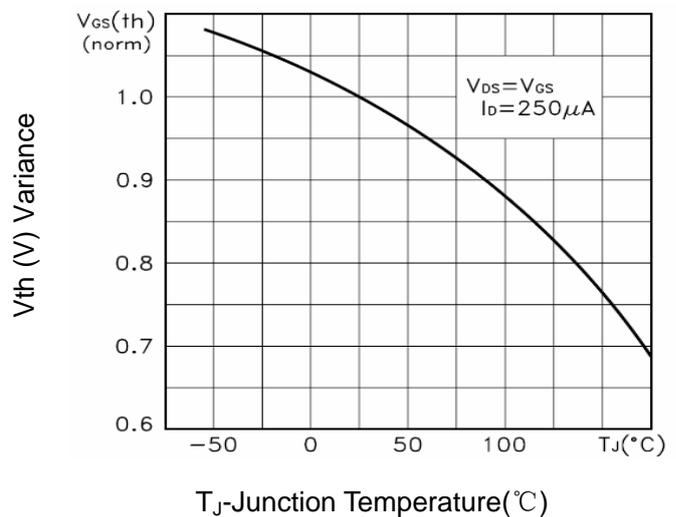


Figure 10 $V_{GS(th)}$ vs Junction Temperature

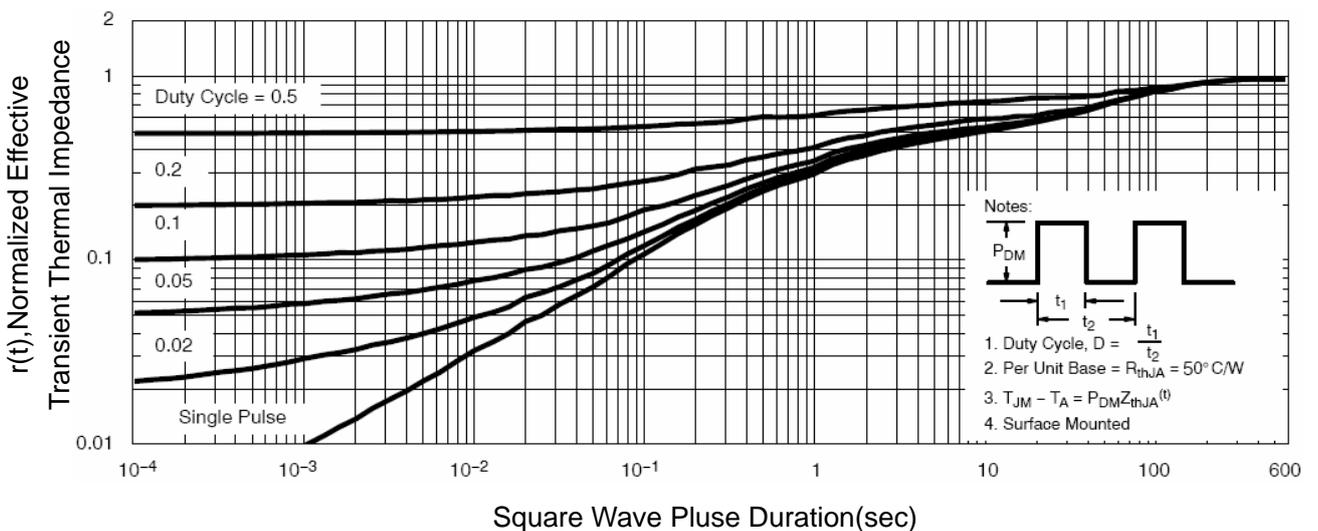
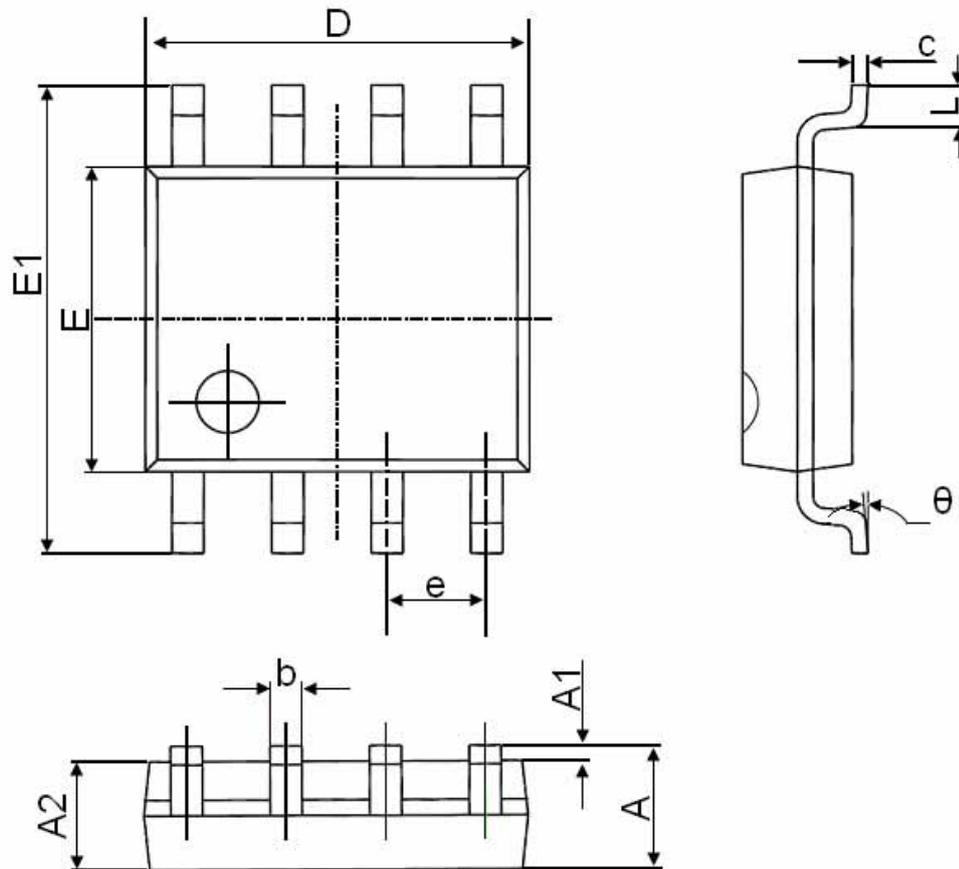


Figure 11 Normalized Maximum Transient Thermal Impedance

SOP-8 Package Information



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	1.350	1.750	0.053	0.069
A1	0.100	0.250	0.004	0.010
A2	1.350	1.550	0.053	0.061
b	0.330	0.510	0.013	0.020
c	0.170	0.250	0.006	0.010
D	4.700	5.100	0.185	0.200
E	3.800	4.000	0.150	0.157
E1	5.800	6.200	0.228	0.244
e	1.270(BSC)		0.050(BSC)	
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°