

20V(D-S) N-Channel Enhancement Mode Power MOS FET

General Features

- $V_{DS} = 20V, I_D = 12A$
 $R_{DS(ON)} < 8m\Omega @ V_{GS}=10V$
 $R_{DS(ON)} < 11m\Omega @ V_{GS}=10V$
- High density cell design for ultra low R_{dson}
- Fully characterized Avalanche voltage and current

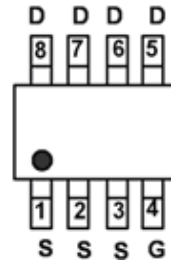


Lead Free

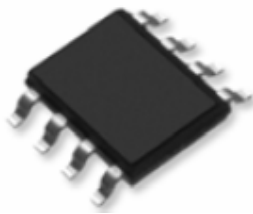
Application

- DC/DC Converter
- Notebook Vcore

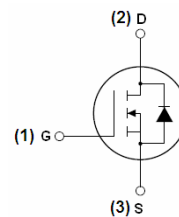
PIN Configuration



Marking and pin Assignment



SOP-8 top view



Schematic diagram

Package Marking and Ordering Information

Device Marking	Device	Device Package	Reel Size	Tape width	Quantity
MSN0212W	MSN0212W	SOP-8	Ø330mm	12mm	2500 units

Absolute Maximum Ratings ($T_A=25^\circ C$ unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	30	V
Gate-Source Voltage	V_{GS}	± 20	V
Drain Current-Continuous	I_D	12	A
Drain Current-Continuous($T_A=100^\circ C$)	$I_D(100^\circ C)$	8	A
Pulsed Drain Current	I_{DM}	40	A
Maximum Power Dissipation	P_D	2.5	W
Operating Junction and Storage Temperature Range	T_J, T_{STG}	-55 To 150	$^\circ C$

Thermal Characteristic

Thermal Resistance, Junction-to-Ambient ^(Note 2)	$R_{\theta JA}$	50	$^\circ C/W$
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Electrical Characteristics (T_A=25°C unless otherwise noted)

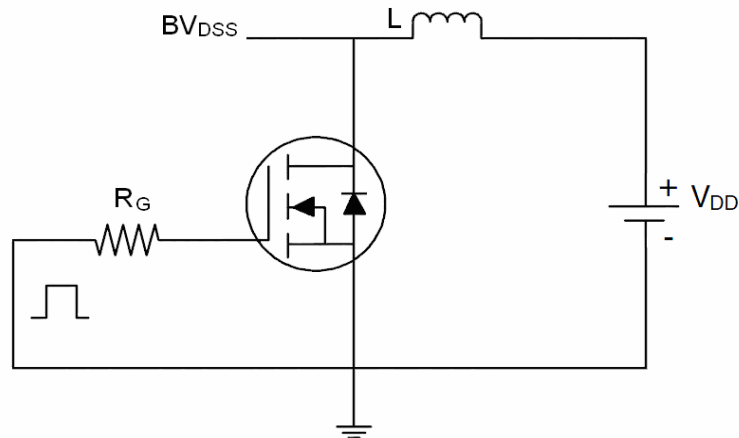
Parameter	Symbol	Condition	Min	Typ	Max	Unit
Off Characteristics						
Drain-Source Breakdown Voltage	BV _{DSS}	V _{GS} =0V I _D =250μA	20	-	-	V
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} =30V, V _{GS} =0V	-	-	1	μA
Gate-Body Leakage Current	I _{GSS}	V _{GS} =±20V, V _{DS} =0V	-	-	±100	nA
On Characteristics (Note 3)						
Gate Threshold Voltage	V _{GS(th)}	V _{DS} =V _{GS} , I _D =250μA	0.5	0.8	1.2	V
Drain-Source On-State Resistance	R _{DS(ON)}	V _{GS} =4.5V, I _D =6A	-	6	8	mΩ
		V _{GS} =2.5V, I _D =5A		8	11	
Forward Transconductance	g _{FS}	V _{DS} =10V, I _D =6A	20	-	-	S
Dynamic Characteristics (Note4)						
Input Capacitance	C _{iss}	V _{DS} =10V, V _{GS} =0V, F=1.0MHz	-	2000	-	PF
Output Capacitance	C _{oss}		-	402	-	PF
Reverse Transfer Capacitance	C _{rss}		-	170	-	PF
Switching Characteristics (Note 4)						
Turn-on Delay Time	t _{d(on)}	V _{DD} =10V, I _D =6A V _{GS} =4.5V, R _{GEN} =1Ω	-	25	-	nS
Turn-on Rise Time	t _r		-	15	-	nS
Turn-Off Delay Time	t _{d(off)}		-	25	-	nS
Turn-Off Fall Time	t _f		-	15	-	nS
Total Gate Charge	Q _g	V _{DS} =10V, I _D =6A, V _{GS} =10V	-	42	-	nC
Gate-Source Charge	Q _{gs}		-	10.8	-	nC
Gate-Drain Charge	Q _{gd}		-	9.2	-	nC
Drain-Source Diode Characteristics						
Diode Forward Voltage (Note 3)	V _{SD}	V _{GS} =0V, I _S =6A	-	-	1.2	V
Diode Forward Current (Note 2)	I _S		-	-	12	A

Notes:

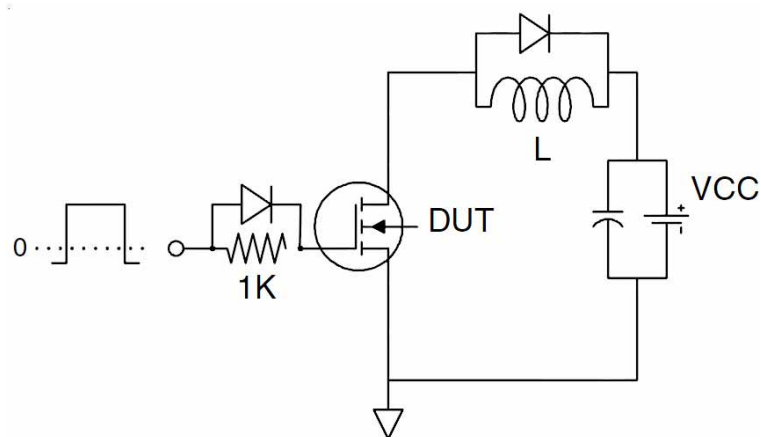
1. Repetitive Rating: Pulse width limited by maximum junction temperature.
2. Surface Mounted on FR4 Board, t ≤ 10 sec.
3. Pulse Test: Pulse Width ≤ 300μs, Duty Cycle ≤ 2%.
4. Guaranteed by design, not subject to production

Test Circuit

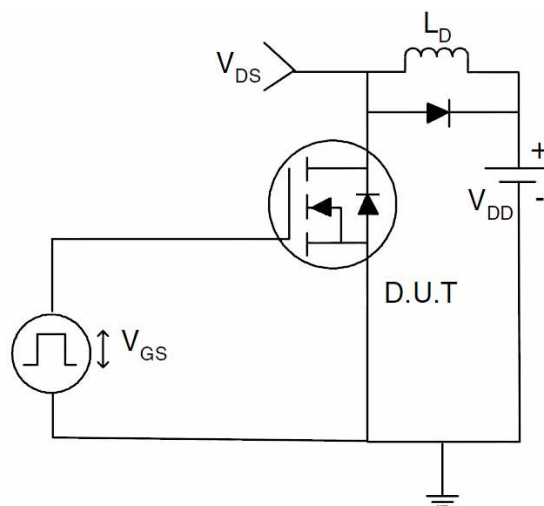
1) E_{AS} Test Circuits



2) Gate Charge Test Circuit



3) Switch Time Test Circuit



Typical Electrical and Thermal Characteristics (Curves)

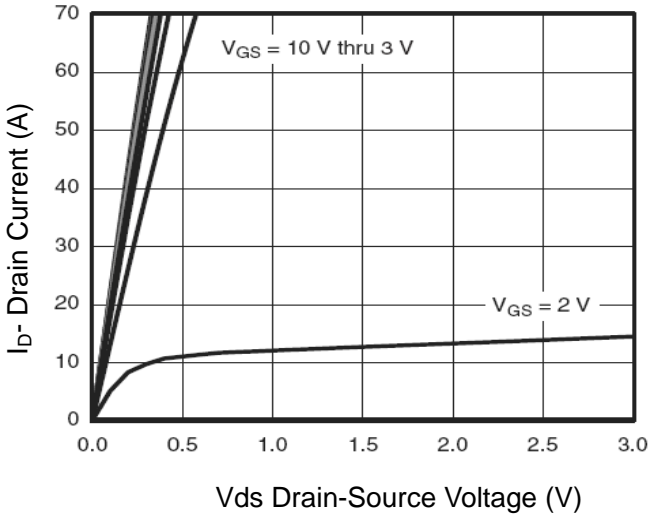


Figure 1 Output Characteristics

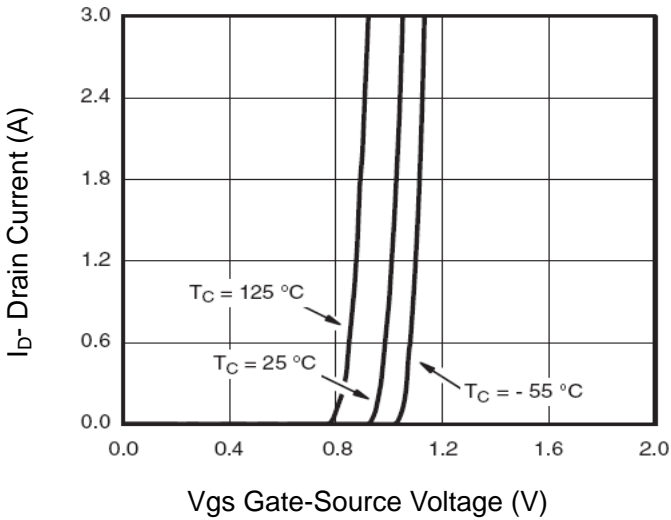


Figure 2 Transfer Characteristics

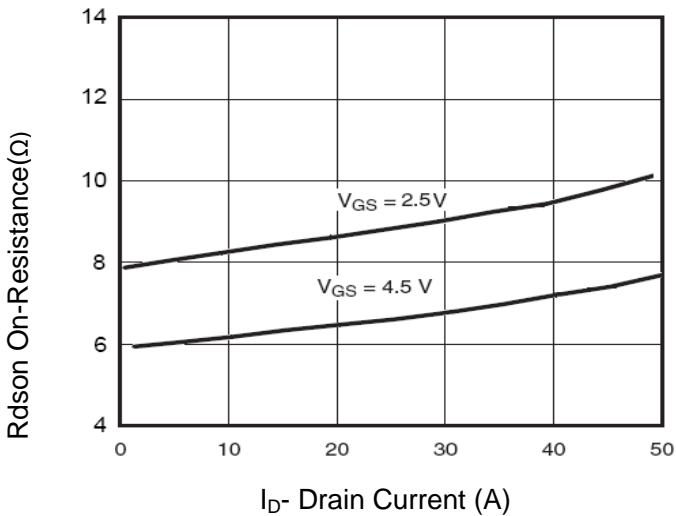


Figure 3 Rdson- Drain Current

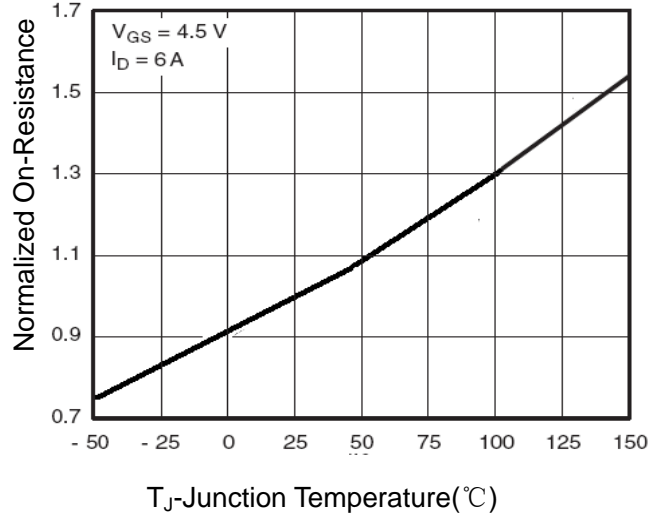


Figure 4 Rdson-Junction Temperature

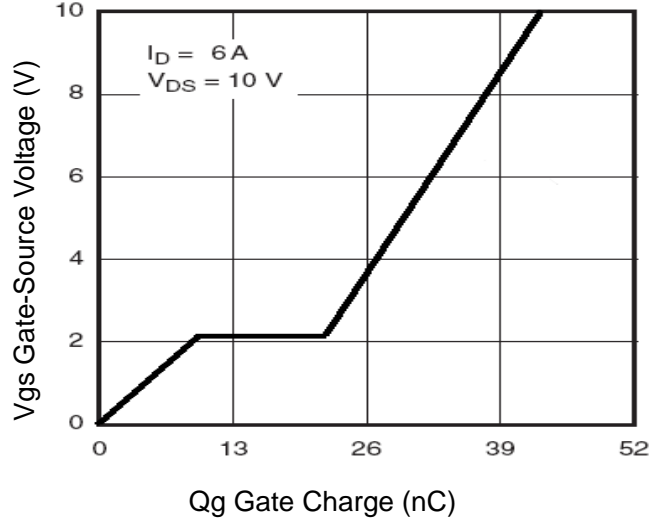


Figure 5 Gate Charge

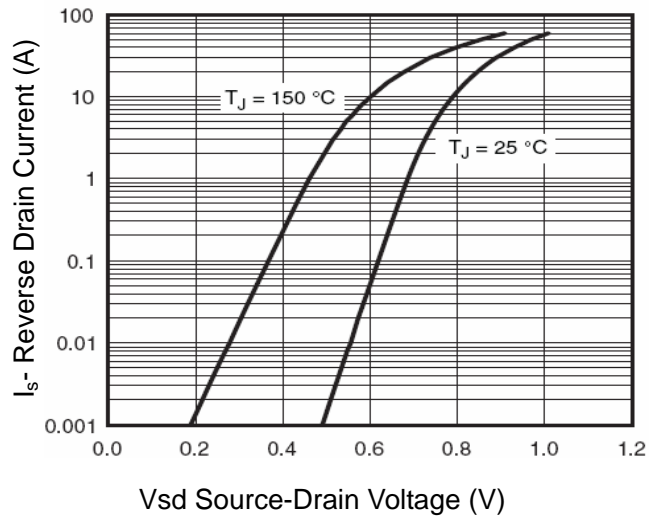


Figure 6 Source- Drain Diode Forward

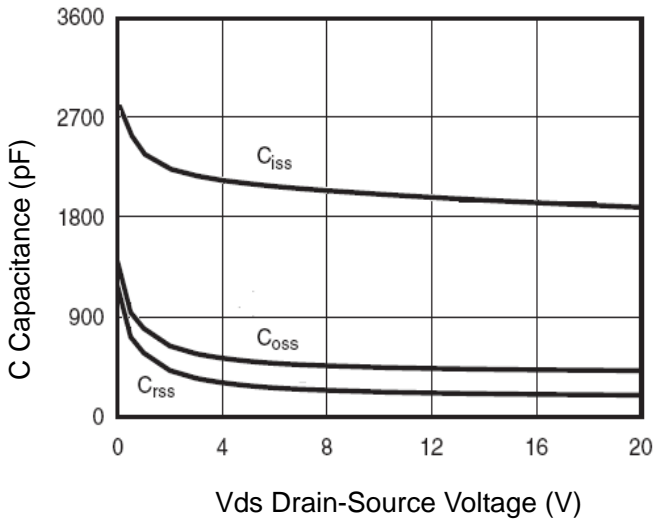


Figure 7 Capacitance vs Vds

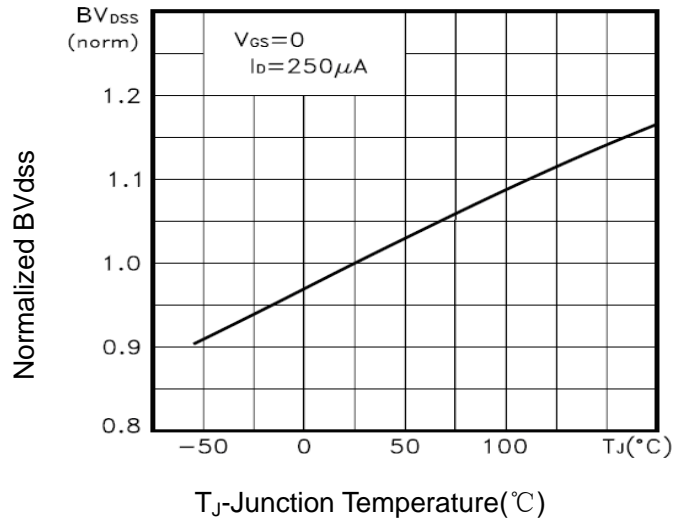


Figure 9 BV_{DSS} vs Junction Temperature

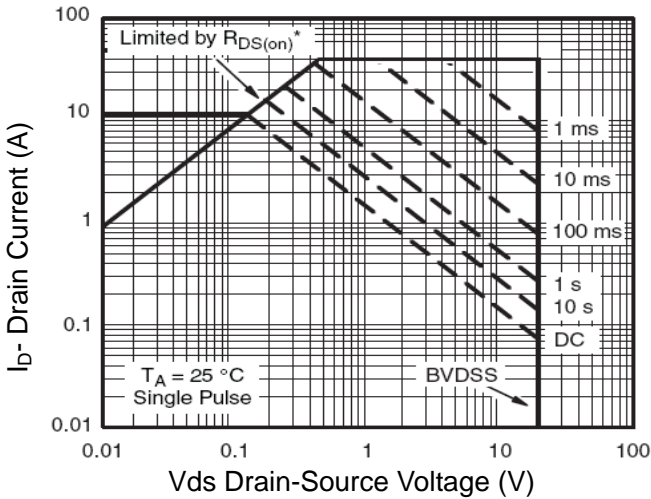


Figure 8 Safe Operation Area

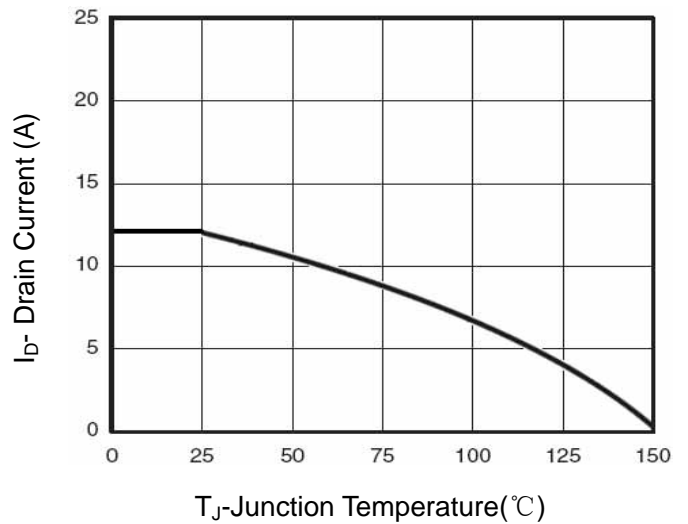


Figure 10 Current vs Junction Temperature

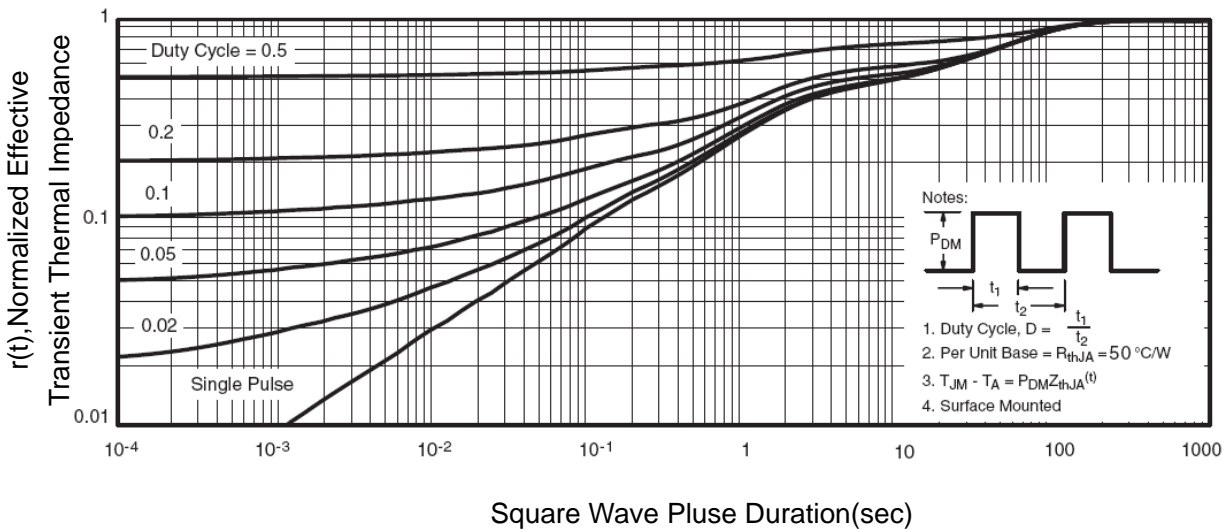
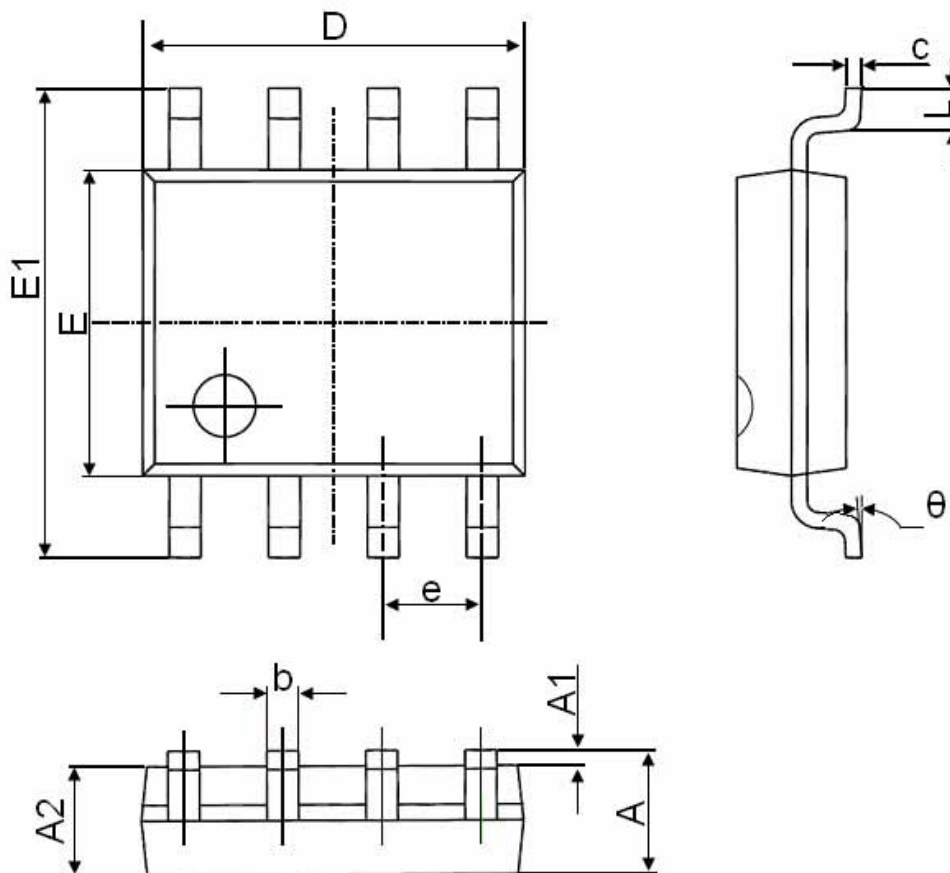


Figure 11 Normalized Maximum Transient Thermal Impedance

SOP-8 Package Information



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	1.350	1.750	0.053	0.069
A1	0.100	0.250	0.004	0.010
A2	1.350	1.550	0.053	0.061
b	0.330	0.510	0.013	0.020
c	0.170	0.250	0.006	0.010
D	4.700	5.100	0.185	0.200
E	3.800	4.000	0.150	0.157
E1	5.800	6.200	0.228	0.244
e	1.270(BSC)		0.050(BSC)	
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°